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Special Lecture
on
CMOS Process Variations: A "Critical Operation Point" Hypothesis

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Abstract:

A brief overview of present and future CMOS process variations will be presented. Prevailing understanding of a chip's behavior under large process variations with statistical delay assumptions leads one to conclude that a small number of errors are likely as we progress further down on Moore's Law. This understanding is challenged by a new hypothesis on the behavior of very large CMOS chips in the presence of process variations. A Thought Experiment is presented which leads to the new hypothesis. The new hypothesis states that in every large CMOS chip, there exist critical operations points (frequency, voltage, temperature) such that it divides the 3-D space (F, V, T) in to two distinct spaces: 1. Error-free operation and 2. Massive errors (i.e. completely inoperable). Two attempts at disproving this hypothesis with real physical experiments will be described. Some consequences of the hypothesis on power savings in large data centers are also suggested.