ABSTRACTS

PH. D. THESES
M. TECH. DISSERTATIONS
M. DES. PROJECTS

- PH. D.

- M. TECH 2002-2004
- M. TECH 2003-2005
- M. TECH 2004-2006
- M. TECH 2005-2007
- M. TECH 2006-2008
- M. TECH 2007-2009
- M. TECH 2008-2010
- M. TECH 2010-2012

- M. DES. 2004-2006
- M. DES. 2005-2007
- M. DES. 2006-2008
- M. DES. 2007-2009

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Introduction

The Resource Centre team is happy to bring out this revised catalogue listing Ph.D. Theses, submitted in 2008 and 2010, M. Tech. Dissertations, submitted by the 2002-2004, 2003-2005, 2004-2006, 2005-2007, 2006-2008, 2007-2009, 2008-2010 and 2010-2012 batch students, and M. Des. Projects submitted by the 2004-2006, 2005-2007, 2006-2008 and 2007-2009 batch students to the Institute. This document covers in all 312 theses and dissertations and are listed in alphabetical order under each year by student's surname. Each entry of the dissertation provides the bibliographical details, such as author (with ID number), title, page numbers, year of submission, supervisor name, call number, accession number, keywords and abstracts. At the end, author and supervisor indexes have been provided to enable the user to locate a specific entry in this catalogue. All these theses and dissertations listed here have also been catalogued in the Resource Centre's Online Catalogue. We have made the effort to bring out this catalogue to supplement the Online Catalogue.

Hope you will find this document useful. We would be happy to have your comments and suggestions, if any, to improve this catalogue further.

Updated on: 18/12/2012 Resource Centre Team

Table of Contents

Ph.D. Theses

M.Tech. Dissertations

2002-2004

Table of Contents

Table of Contents

2003-2005

Table of Contents

Table of Contents

2004-2006

Table of Contents

Table of Contents

Table of Contents

2005-2007

Table of Contents

Table of Contents

2006-2008

Table of Contents

Table of Contents

2007-2009

Table of Contents

Table of Contents

Table of Contents

2008-2010

Table of Contents

Table of Contents

2010-2012

Table of Contents

M. Des. Projects

2004-2006

2005-2007

2006-2008

2007-2009

Table of Contents

Indices

Ph. D. Theses

(Abstracts)

Author: Laliwala, Zakir (200221003)
Title: Event-driven Service-oriented Architecture for Dynamic Composition of Web Services; 184 p.; 2008.
Supervisor: Chaudhary, Sanjay
Call No.: 004.36 LAL
Acc. No.: T00193
Keywords: Computer architecture; Service-oriented architecture (Computer science); Service-oriented computing; Discrete-time systems; Business -- Data processing; Business enterprises -- Computer networks; Computational grids (Computer systems); Web services; Semantic Web; Web services – standards; Electronic data processing -- Distributed processing; Management information systems; Thesis, Doctoral Degree.

Abstract: The Business process contains a set of services to fulfill its goal. The Service is a software component to perform a specific activity of a business process. The Business processes are event-driven and change frequently during the life cycle of a process. The state of services should be managed for proper integration during the execution of a business process. Core Web services standards are stateless and do not support event and notification. In today's dynamic environment, changes in business process requirements, terminologies, technologies and policies need to be reflected in the software systems. To provide seamless interoperable integration, automation, execution monitoring, state and notification management of a dynamic business process, scalable software architecture is required.

This thesis proposes event-driven service-oriented architecture by converging the Web services, Semantic web, and grid computing; to model, compose, deploy and execute event driven dynamic business process. Web service provides loosely coupled integration of information and services for orchestration of a business process. Semantic provides interoperable integration, automated orchestration, negotiation, content based service selection and composition of a business process. Grid business process supports state, notification, service grouping, and policy. Grid provides required middleware support for the execution of a stateful and event-driven dynamic grid business process. We propose event calculus based formal approach for event-driven modeling and rules based approach for dynamic composition. As for the proof-of-concept, agro-produce marketing process is considered. Research experiments are performed using existing open standards, specifications, and tools to realize event-driven service-oriented architecture and its lifecycle.

Author: Sorathia, Vikram (200221005)
Title: Dynamic information Management Methodology with Situation Awareness Capability; xv, 337 p.; 2008.
Supervisor: Chaudhary, Sanjay
Call No.: 658.4038 SOR
Acc. No.: T00194
Keywords: Information management ; Management information systems; Human-computer interaction; Semantic networks (Information theory); Knowledge management; Human-machine systems – Design; Awareness; Information organization; Information technology – Management; Electronic data processing -- Distributed processing; Distributed databases; Database management; Thesis, Doctoral Degree.

Abstract: In present world, information generation, handling and utilization is deeply integrated with various

activities. From entertainment to serious professional activities, information content is managed in some ways. Appropriate information content is beneficial and sometimes becomes critical to life, business or the environment that supports them. Handling of information is therefore increasingly perceived as integral part of the activities. Systematic approach for handling information by individuals and organization is known as "information management".

A common approach towards information management is limited to recording and retrieval of data pertinent to various human activities or environmental processes. The resulting system acts as a computerized log of human activity transactions or phenomena recorded in natural environment. Systems supporting information management are defined based on project specific requirements with limited scope. The project-oriented or mission-specific engineering approaches employed in designing such systems also restrict the scope of supported information management activities.

It is important to realize that projects or missions are identified only as short-term objective that contribute to the long-term goals and vision of entities. A system defined to serve shortterm goals may soon become incapable of meeting the emergent needs. Even with accurate estimation of potential change, external intervention cannot be avoided due to dependence of knowledge, authority and resource capability required to realize the goals. The dynamism exhibited by relevant entities, results in continuous change of needs resulting in constantly changing requirements.

With increasing amount of complex interdependence and dynamic behavior of relevant entities, the task of information management has become difficult. From the scale of effort required to address the complex interdependence, it is realized that information management cannot be carried out with systems created and managed by individuals and organizations in isolation. Also, from the dynamic behavior and evolution exhibited by relevant entities, it is realized that underlying systems must also undergo change at similar rates. In summary, a paradigm shift is required in information management strategy and information should be made available as critical infrastructure service.

This thesis argues that information management should be based on the goals of the involved individuals instead of the conventional activity-oriented approaches. The required approach not only should support the goal-specific information, but also allow identification of newer goals with emerging trends in the system. Information need of individuals and organizations is vi uniquely identified in the form of situations. The state of having access to relevant information is defined as situation awareness capability. The situation awareness approach proposed for information management strategy identifies role of individuals in producing and consuming information. It is based on the realization that, no one can have the global picture of the situation, but can play a role in building the rich picture of situation by contributing the part of the situation known. The resulting coordinated effort allows realization of situation awareness capability to the contributors.

In order to support the argument, the situation theory and semantics is accepted as base. It is stated that small coordinated assertions regarding situations can be integrated to prepare a rich representation of the world. Qualitative and quantitative estimate of information needs are identified based on the commitment towards goals. Three problems are identified in identification of information needs of individuals and organizations. The implied goal-matching problem relates to the challenge of identification and handling of goals that are not explicitly expressed. The transient system element problem indicates the challenges of numerous short-lived entities that are relevant to the information needs. The third problem is regarding identification of the event space, a set of all possible events that are possible in given scenario.

As a solution to this problem, a conceptual modeling strategy followed by information processing strategy is proposed. The proposal utilizes the rich representation created with conceptual modeling process in meeting the information needs. It is established that scale and scope of work involved in conceptual modeling and information processing requires large-scale collaboration from various stakeholders. For consistency of collaborative effort, appropriate method content is provided. Reuse and traceability of work products are encouraged with unique situation awareness artifacts furnishing information about task and availability of reusable outcomes and other related information. The proposed information management facility is prescribed as a critical infrastructure service required in achieving the large-scale collaboration. Appropriate system architecture is introduced to facilitate realization of required domain specific middleware services.

Author: Bombale, Uttam Laxmanrao (200321001)

Title: Broadband Microstrip Antennas with Switchable Polarizations; 149 p.; 2010.

Supervisor: Gupta, Sanjeev

Call No.: 621.3824 BOM

Acc. No.: T00240

Keywords: Microstrip antennas; Antenna arrays; Broadband communication systems; Ultra-wideband antennas; Dual-polarization; Cross-polarization; Phased-array antenna; Microwave circuits -- Design and construction.

Abstract: Microstrip antenna consists of a patch of metallization on grounded substrate. These are low profile, lightweight antennas, most suitable for aerospace and mobile application. They are replacing many conventional antennas used in defense and commercial applications. They have got certain drawbacks such as narrow bandwidth, low gain, and low power handling capability and polarization impurity. Many researchers are trying to overcome these drawbacks.

In this thesis also some efforts have been done to overcome certain drawbacks of microstrip antenna. One of the serious limitations of the microstrip antennas is its narrow bandwidth. The impedance bandwidth of MSA is around 1% only for thin substrates. The bandwidth of the MSA can be increased by increasing thickness of the substrate. If the thickness is increased it creates problems for impedance matching, produces radiations from the feed and distortions in the radiation patterns due to higher order modes. Therefore to avoid these problems thicker substrate is not used. The common techniques to improve bandwidth are Planner multiresonator configurations, Electromagnetically coupled MSA; Aperture coupled MSAs, Impedance matching networks for broad band MSAs & Log periodic MSA configurations. It is advantageous to use Electromagnetically coupled MSA because of its small size and no back radiations. Therefore Electromagnetically coupled MSA is used to design the antenna. The MSA gives linear polarization. Many times we need circular polarization with low cross polar level (generally below 10-12 dB). This circular polarization is obtained in this antenna using a shorting pin. This is the major achievement. Many papers discuss about bandwidth only, a few papers discuss just about polarizations using shorting pins.

Many times we need large bandwidth, desired polarization and high gain. In order to obtain high gain we have to form an array of antennas. It is convenient to feed the array elements using microstrip feed. Therefore the Electromagnetically coupled MSA is fed using a microstrip line as described in chapter 4. Some times we need right circular or left circular or linear polarization depending on situation. These polarizations can be obtained using two shorting pins instead of one as described in chapter 4.

In satellite TV transmission vertical and horizontal polarizations (Eθ and EΦ) are used. In order to minimize adjacent channel interference they are placed alternately on vertical and horizontal polarizations. These additional Eθ, EΦ polarizations as well as RHCP and LHCP are obtained using additional shorting pins as described in chapter 4. for satellite TV transmission we need high gain around 30 dB. This can be obtained using an array of above elements. The design is given in chapter 4. Various feeding techniques, transmission lines, bends, power dividers and quarter wave transformers are discussed. Spacefed microstrip antennas are also designed, simulated and studied in chapter 5.

Recently fractal antennas are becoming very popular because of their small size, multiband response and high efficiency. The basic types of fractal antennas are designed and simulated in chapter 6. Bandwidth is the major problem in microstrip antennas. In chapter 7, it is discussed how do we get large bandwidth, and the concept is used to obtain very large or ultra-wide bandwidth using rectangular microstrip antenna. The same concept is used to obtain very large bandwidth using sierpinski fractal antennas.

Author: Guntuku, Dileepkumar (200421002)

Title: Micro-level Drought Preparedness with Information Management and Rural Knowledge Centres: A Framework to Support Rural Farm Families

Supervisor: Balaji, V. and Chaudhary, Sanjay

Call No.: 363.349297 GUN

Acc. No.: T00241

Keywords: Droughts; Drought forecasting -- Queensland; Water-supply -- Risk assessment; Water-supply -- Risk assessment -- Case studies; Risk management; Environment policy; Case studies; Statistics; SCORM; Content Management; ICT applications

Abstract: Drought and desertification are serious problems that significantly affect hundreds of millions of people and ecosystems. When drought occurs, the farm communities are usually the first to be affected because of their heavy dependence on the stored soil water. If the rainfall deficiencies continue, even people who are not directly engaged in agriculture will be affected by drought. This underscores the vulnerability of entire societies to this phenomenon; this vulnerability varies significantly from one nation to another. Although crisis management approach is routinely followed approach for providing relief, the studies on drought, carried out in different parts of the world, suggested that preparedness is better than relief and information is backbone of drought preparedness. However, the efforts have been taken for generating micro-level drought assessment and early warning is least understood until recent years. It was therefore, in this study, an attempt has been made to develop a micro-level drought preparedness framework to support rural farm families.

The established practices such as Sources of Agricultural Information management (International/National/Extra-Institutional), Information and Communication Technology (ICT) Enabled Rural Knowledge Centres (RKC), Open and Distance Learning Methods, micro-level drought assessment and early Warning technique have been identified as key components in developing such framework. These components were considered as the objectives of this research study, and conducted series of studies and experiments to understand the existing approaches and needed arrangements in defining and developing proposed framework. For each finding reported in the experimental objectives, a clear chain of evidence was established supported also by interview statements. The individual micro-level drought preparedness framework components were integrated carefully, based on the series of findings, systemic analysis of the data and the continuous interpretation of the observations, to develop the proposed framework.

The study concludes that the proposed framework has shown a way to improve micro-level drought preparedness by bringing various ICT tools, information management techniques, open learning approaches, and micro-level drought assessment technique under one umbrella with an intermediary entity called ICT enabled RKCs owned and run by rural farm families. The usability evaluation studies on individual components revealed that the approaches such as these will have implications in planning micro-level drought preparedness strategies. The vulnerable rural families now have the means to estimate their own vulnerability and can use the information available at ICT enabled RKCs to make more informed decisions, which offers a sounder basis for designing drought preparedness and adaptation strategies.

M. Tech. Dissertations (Abstracts)

2002-2004

Author: Acharya, Jaykumari (200211020)
Title: Classification of Quantum Cryptography; x, 104 p.; 2004.
Supervisor: Jadhav, Ashish
Call No.: 005.82 ACH
Acc. No.: T00013
Keywords: Ciphers; Cryptography; Quantum cryptography.
Abstract: Modern Classical Cryptography is divided into two parts. The first part is Asymmetric (public-key) cryptography and the second is Symmetric (private or secret-key) cryptography. In spite of its popularity public-key cryptography has major flaws. Fast factoring algorithms or computers with fast processing power can break the public-key cryptographic system. In the case of private key cryptography, it is expensive to distribute the key via a trusted carrier or personal meetings. So, to overcome these drawbacks of classical cryptography, a cryptographic scheme based on the principles of quantum physics was developed. Quantum Cryptography provides unconditional security. Quantum cryptographic systems are provably secure systems that uses public channel for the distribution of the secret key. To get unconditional security quantum cryptography uses the principles of quantum physics like No-cloning theorem, Heisenberg's uncertainty principle and quantum entanglement. Here, Classification of Quantum Cryptography is proposed. Quantum Cryptography is an alternative for the Classical Cryptography especially to have unconditional security. Classification may help the designer for an appropriate choice of the quantum cryptographic techniques.

Author: Agarwal, Shivani (200211001)
Title: An Improved Algorithms for Modular Multiplication and its Application to Block Cipher RC6; v, 87 p.; 2004.
Supervisor: Mathuria, Anish
Call No.: 005.82 AGA
Acc. No.: T00001
Keywords: Algorithms; Block ciphers; Ciphers; R6 Ciphers.
Abstract: This thesis explores the area of hardware implementation of block ciphers. An algorithm for modular multiplication is proposed which is efficient in terms of speed and area. To demonstrate the effectiveness of the algorithm an implementation of RC6 cipher using the proposed algorithm is made and compared against the existing implementations.

Author: Athale, Suprita (200211035)
Title: A Fractal Based Approach for Face Recognition; 44 p.; 2004.
Supervisor: Mitra, Suman K.
Call No.: 006.4 ATH
Acc. No.: T00026
Keywords: Computer vision; Face recognition; Fractals; Image compression; Pattern recognition systems; VLSI systems.
Abstract: An automated face recognition system is proposed in this dissertation. The system efficiently recognizes a candidate (test) image using the interdependence of the pixel that arises from the fractal compression of the image. The interdependence of the pixels is inherent within the fractal code in the form of chain of pixels. The mechanism of capturing these chains from the fractal codes is called pixel chaining. The present face recognition system tries to match pixel chains of the candidate image with that of the images present in the database. The work domain of the

system is fractal codes but not the images. This leads to an advantage towards handling large database of face images.

The system performance is found to be very satisfactory with the recognition rate of 98.4%. A minor improvement in the performance of the system over a few existing methods has been observed.

Author: Bavishi, Hardik N. (200211038)
Title: Performance Analysis of MPEG traffic under Deficit Round Robin Scheduler; xi, 71 p.; 2004.
Supervisor: Jotwani, N. D.
Call No.: 621.388 BAV
Acc. No.: T00029
Keywords: MPEG; Robin Scheduler; Video coding standard; Video compression.
Abstract: The use of network multimedia applications like Video Conferencing and Video-on-Demand is likely to increase tremendously in future. Bandwidth, delay and delay variation are important performance parameters in such multimedia applications. The multimedia traffic, typically bursty in nature, can be represented by MPEG traffic. MPEG being one of the most popular video-encoding standards, the MPEG traffic will have to be very carefully handled by the network so as to satisfy its performance requirements. Scheduling is a key mechanism in packet-switching networks. Performance achieved by an application depends on how its traffic is treated along its path through the network. When packets of traffic belonging to an application are waiting for transmission at an intermediate node, the scheduler at the node decides their order of transmission. During congestion, the scheduler decides which packets to drop. Thus the scheduler decides how the network resources (link bandwidth and buffer space) are shared among the flows. Fair schedulers are those, which allow fair sharing of these resources among the flows. Deficit Round Robin (DRR) is one such popular and efficient fair scheduler. The main performance parameters of interest are delay and delay variation. We identify and define the factors that impact performance achieved by a flow under DRR. We design simulation experiments based on the identified factors to understand and analyze the effects of the factors on performance. Based on this we analyze performance of the MPEG traffic under DRR scheduler in presence of best-effort traffic. DRR++ is a modification of DRR to handle bursty latency critical traffic preferentially in the presence of the best-effort traffic. We also obtain similar simulation results for DRR++ to understand the improvement in performance achieved by the MPEG traffic.

Author: Bhatt, Amee (200211034)
Title: Performance Analysis of DiffServ Multicast (DSMCast) for Heterogeneous Multicast Receivers; ix, 75 p.; 2004.
Supervisor: Jotwani, N. D.
Call No.: 004.678 BHA
Acc. No.: T00025
Keywords: DiffServ multicast; Heterogeneous receivers; Internet; QoS architecture; World Wide Web, WWW.
Abstract: Internet is a large infrastructure that provides means for global communication. One of the biggest challenges faced in its growth and maintenance is the provision for the best Quality of Service (QoS) to the end-user applications. There exist some mechanisms that have evolved to achieve QoS in IP networks and amongst them Differentiated Services (DiffServ) is a prevalent one. With the increased usage of multimedia applications such as video and audio conferencing, which primarily use multicast mode of communication, one obvious question that arises is whether suitable QoS in terms of resource assurance and service differentiation can be guaranteed to them. This thesis answers the question affirmatively and discusses a recently proposed approach: DSMCast, which attempts to offer QoS for multicast applications in DiffServ domain.

The main objective of the thesis is to analyze how DSMCast provides support for heterogeneous QoS receivers participating in a multicast session. The performance analysis of DSMCast indicates that it can support the heterogeneous QoS requirements for the multicast receivers in a better way than traditional IP multicast. The simulation results bring out an important implication due to

the nearness of receivers who have low QoS demands to those who have high QoS demands.

Author: Desai, Vishal (200211029)
Title: A Novel Approach for Localization in Ad-Hoc Sensor Networks; 51 p.; 2004.
Supervisor: Ranjan, Prabhat
Call No.: 681.2 DES
Acc. No.: T00021
Keywords: Ad-hoc sensor networks; Routing; Sensor networks.
Abstract: The ability of a sensor node to move itself or to otherwise influence its location will be critical in sensor networks. Today, the wireless community is putting great effort on the possibility of deploying thousands of tiny sensors all over the place and measuring all kinds of data within. Sensor network is a network of small devices, collaborating with each other to produce a larger sensing task. Most of the current literature on location discovery in wireless and sensor networks assumes the availability of GPS receivers at some nodes or beacon nodes with known position. But as we know having a GPS receiver at sensor nodes may not be feasible due to the limitations of satellite coverage inside the building or due to cost reasons. Further for ad hoc deployment of nodes, it is unreasonable to assume the presence of beacon nodes with prior position information. Hence, the main objective behind this research work is to introduce a localization/positioning method that would be GPS-free and beaconless, and finally we come up with a method called "LRT - Localization using Routing Table" which is also scalable, distributed and able to support the ad hoc deployment of large-scale sensor networks quickly and efficiently.

Author: Dixit, Parth (200211032)
Title: Representation Theory in Signal Processing: Some Connections Through GAP; vi, 79 p.; 2004
Supervisor: Sinha, V. P.
Call No.: 621.3822 DIX
Acc. No.: T00064
Keywords: Groups; Representation of groups; representation theory; Signal processing.
Abstract: This thesis is concerned with the study of some of the recent developments in the area of signal processing that arise from the connections of discrete transforms and their inherent symmetries with the representation theory of groups. There are two main aspects of these developments, one, that of unification and generalization and, two, that of constructing fast algorithms for the implementation of matrix transforms.

The focus of this thesis is on the second line of developments — that of constructing fast algorithms. The central theme of recent work in this direction is that of defining symmetries of a transform in terms of a pair of group representations, and then decomposing the representations along a chain of subgroups. Such a decomposition leads to a factorization of transform matrices into product of sparse matrices, which provide a means of fast transform computations.

The decomposition process relies on results of group representation theory not commonly familiar to workers in the area of digital signal processing. Furthermore, the algebraic computations involved would be enormously difficult without the use of computer algebra tools and software packages of recent origin whose potential is only now beginning to be realized.

On both counts, there is a need for providing a bridge between what is commonly understood of fast transforms and what the recent developments mean for them. With this need in mind, an attempt has been made in this thesis to (a) identify and discuss the relevant representation theory results, and (b) present results of hands-on experience, in the form of examples, with the software package called GAP (acronym for Groups, Algorithms and Programmes) in transform factorization.

Author: Gajjar, Mrugesh R (200211005)
Title: Processor Allocation for Parallel Applications In Computing Cluster; viii, 36p.; 2004.
Supervisor: Jotwani, N. D.

Call No.: 004.35 GAH

Acc. No: T00003

Keywords: Cluster computing; Computing cluster; Distributed shared memory; Multi-processors; Parallel processing; Processor allocation.

Abstract: We study the problem of processor allocation in multi-computer for parallel processes that do I/O and IPC (Inter Process Communication). A simulator has been modified to accept synthetic parallel workload that does I/O and IPC. We study the effect of I/O and IPC on performance of parallel applications using the simulator. Also, we study a novel design approach for distributed operating system Kerrighed, which uses kernel level distributed shared memory to provide global resource management of CPU, memory and disks and efficient process migration mechanism. As kernel level distributed shared memory provides unified basis for doing IPC we study the special case of processes, which communicate using underlying DSM. We propose to use state of the DSM pages in scheduling decisions and utilize efficient process migration mechanism to reduce consistency related communication in DSM and thereby improve the response time of parallel processes.

Author: Hashey, Jitendra Prabhakar (200211015)

Title: Design of CMOS Front end for 900MHz RF receiver; vii, 98p.; 2004.

Supervisor: Bhat, Amit

Call No.: 621.3815 HAR

Acc. No.: T00009

Keywords: Circuit design; Complementary metal oxid semiconductor (CMOS); CMOS; Radio frequency; RF receiver; Simulation.

Abstract: Portable wireless personal communication systems such as cellular phones, message pagers, and wireless modems traditionally have been built from a mixture of IC technologies. In fact if we section a commercial cellular phone, we could find many separate ICs together linked in the analog section. Moreover some of these ICs are realized on GaAs substrate, others on bipolar Silicon and only the digital section is integrated on CMOS substrate. One of the main challenges facing complete integration of receiver (transmitter) hardware has been a lack of suitable on-chip RF and IF filtering. This approach increases system complexity, cost, and power consumption. The aim of this thesis consists in the investigating the characteristic of RF building blocks that constitute an integrated RF receiver. This thesis, is the balance between microelectronic and microwave, and investigates the bottlenecks in the fully integration of an RF receiver, and is particularly focused on the design of high quality passive devices and high performance low noise amplifiers.

This receiver is part of a single chip transceiver, which operates in the 902-928 MHz ISM band. The receiver combines a balanced low-noise amplifier; down conversion mixers, low pass channel-select filters, and IF amplifiers all in one single CMOS IC. Noise components of MOS at high frequencies were studied in detail. Device properties unique to CMOS are exploited to obtain highly linear RF circuits.

In design of low noise amplifier, I concentrated my efforts on minimizing the value of passive devices so that all of them can be fabricated on single chip. For this I undertook several optimizations and tradeoffs. Particularly the noise power trade-off with inductors value was stressed on. LNA had three primary design specifications of input impedance matching, gain and noise. I also experimented on several techniques of input match. The results obtained are suited to the needs fairly well. In the mixer design, my primary goal was to design a doubly balanced mixer for single ended inputs. This was necessitated because the antenna signal received was single ended before the LNA and even in LNA, due to several considerations; I obtained a single ended output. Finally this report contains all my designs and simulation results.

Author: Jadia, Pawan K. (200211023)

Title: Energy efficiency secret aggregation for wireless sensor networks; v, iii, 70p.; 2004.

Supervisor: Mathuria, Anish

Call No.: 681.2 JAD

Acc. No.: T00016

Keywords: Sensor networks; Wireless LANs; Wireless sensor networks.

Abstract: Sensor networks involves large amount of nodes spread over a region. Data aggregation is an important technique for reducing the amount of data to be transmitted in the networks. Data confidentiality is a crucial requirement in many applications. Many existing protocol for secure aggregation do not provide confidentiality. To reduce the computations, it is desirable to have a protocol in which aggregation can be done without decrypting the data at intermediate nodes. This thesis proposes a protocol in which nodes can do data aggregation without learning the neighboring nodes data. The scheme is based on Processing Over Encrypted Data. Much work has been already done in various fields using this cryptographic construct but to the best of our knowledge the field of sensor networks is still untouched. Using this construct in the field of sensor network will be a novel idea because it leads to energy efficient secure aggregation and can open new directions of research in the field of wireless sensor networks.

Author: Jain, Nikhil (200211024)

Title: Design and implementation of a framework for context aware mobile services; xii, 100 p.; 2004.

Supervisor: Srivastava, Sanjay

Call No.: 621.38456 JAI

Acc. No.: T00017

Keywords: Cellular telephone systems; context aware mobile service; FCAMS (Framework for Context Aware Mobile Service); Mobile service.

Abstract: Applications designed for mobile platforms are traditionally hampered by the limitations of the client devices, in particular limited user interface and the change of user environment due to mobility. Incorporating location of the device, and more generally the whole context of the user and device in the computation has clear advantages. A framework for context aware mobile services (FCAMS) targeted for cellular data network is proposed. We provide a detailed architecture of the framework. The design provides a generic way to add context to the mobile applications. An implementation of the framework along with an example service, ATM Finder is done. Functional analysis of the implementation is performed.

Author: Jindal, Gaurav (200211026)

Title: Design and Implementation of Network Intrusion Detection System; vii, 68p.; 2004.

Supervisor: Srivastava, Sanjay

Call No.: 621.38224 JIH

Acc. No.: T00018

Keywords: Communication network architecture; Computer networks; Electronic interference; Internet security; Network intrusion detection system.

Abstract: Most of the intrusion detection systems are based on matching signatures or rules. These rules are the patterns that define the possibility of occurrence of attack. Such signature based intrusion detection system look at incoming events and match these events against the signature rules to detect known attacks. We propose a generic model of Network Intrusion Detection System (NIDS) that includes a signature definition language, signature based detection engine and alert generation and prevention schemes.

This generic model is based on signature classification techniques employed by current signature based NIDS architectures in which signatures are stored in main memory in the form of non-optimized tree or multi link list structures.

At high-speed, techniques employed by signature-based systems become inefficient resulting in performance degradation of NIDS. We have applied clustering and classification algorithm based on decision tree for efficient signature matching. The decision tree classifier approach creates tree from the signature features and its discrete set of values. Decision tree classify the signatures

based on features such that each of the signature could be classified either as individual or group identity.

We have compared the performance of signature detection engine based on linear as well as decision tree classification. In particular we have shown that tree based classifier outperforms the link list structure by a factor of 4 to 5 when tested by reading sample data from tcp dump files and also the tree classifier has more % of throughput at

high data traffic. The % detection varied from 72 % to 30% for tree approach while for linear model % detection varied from 52 % to 30% when packets were flooded at the rate of 4000 to 16000 packets/sec that clearly indicates that linear classifiers dropped more number of packets.

For multi packet inspection we compared sequential based threshold method, adaptive threshold method and cusum algorithms and found that adaptive threshold method and cusum method performs better than sequential time based method in terms of producing less number of false alarms.

Author: Londhe, Tushar (200211028)
Title: A Fractal Based Approach for Image Segmentation; viii, 53 p.; 2004.
Supervisor: Banerjee, Asim
Call No.: 006.42 LON
Acc. No.: T00020
Keywords: Fractals; Image processing; Image reconstruction; Image segmentation; Pattern recognition.
Abstract:

In this thesis, we have proposed an algorithm for image segmentation, using the fractal codes. The basic idea behind this algorithm is to use fractal codes for the image segmentation. This method uses compressed codes instead of the gray levels of the image. Therefore it is cost effective in the sense of storage space and time as no decoding is performed before using the segmentation algorithm. Moreover, the proposed scheme can directly use on the images accessed from the image database where images are kept in fractal-compressed code.

Author: Mehta, Shalin (200211004)
Title: On Wavelets and Fractal Modulation; xiii, 80 p.; 2004.
Supervisor: Sinha, V. P.
Call No.: 625.3822 MEH
Acc. No.: T00002
Keywords: Fractal modulation; Fractals; Wavelet based signal processing; Wavelets.
Abstract:

The thesis considers a communication problem - that of communicating over a channel having simultaneously unknown bandwidth and unknown duration. As a solution to this problem, the thesis looks into a modulation scheme - Fractal Modulation - proposed by Gregory Wornell and Alan Oppenheim.

Wornell and Oppenheim have observed that requirements of reliable communication over such a channel can be met using 'scale-diversity' (transmitting the information at multiple time-scales). To achieve this scale-diversity, they have proposed the use of a particular class of self similar signals, called bihomogeneous signals. They have developed an inner product space representation of bihomogeneous signals. This representation stems from dyadic orhthonormal wavelet based expansion of bihomogeneous signals. Apart from providing very natural and convenient framework of signal representation, these wavelet based expansions lead to efficient algorithms for analysis and synthesis of these signals.

This thesis critically analyzes links between important concepts of the general communication problem, the bihomogeneous signal model and wavelet based signal-processing methods. In the process, we have been able to achieve an understanding of the role of bihomogeneous signals and wavelet-based signal processing techniques in providing elegant and efficient solution to this unconventional problem. During the course of the thesis, we could implement and simulate the transmitter part of the complete communication system (transmitter, channel model and

receiver). MATLAB was used for this purpose. The thesis presents implementation and simulation of algorithms for synthesizing channel waveform for Fractal Modulation scheme. The results of the simulation corroborate those expected from theoretical treatment.

Author: Mishra, Mayank (200211027)
Title: Physical and Logical Mobility of CORBA Servants under Intermittent Connectivity Nomadic Environments; x, 114 p.; 2004.
Supervisor: Chaudhary, Sanjay
Call No.: 005.276 MIS
Acc. No.: T00019
Keywords: Common object request broker architecture (CORBA); CORBA; Middleware technologies; Mobility layer; Object-oriented middleware.
Abstract:

In a wired environment, object-oriented middleware facilitates the development of distributed objects. Common Object Request Broker Architecture is a prominent example of object-oriented middleware. As a joint effect of advancement in electronics and telecommunication manufacturing segments and tremendous increase in the demand of new class of services from mobile devices by mobile device users, middleware technologies can empower mobile devices by providing significant platform for many services. Object-oriented middleware are not inherently designed to support wireless environment behaviour. The aim of this research is to investigate the issues of the Object Management Group's Common Object Request Broker Architecture (CORBA) to facilitate application-to-application communication in wireless environment where connectivity is intermittent. The dissertation discusses the issues in the design and implementation of architecture where CORBA objects have migrating behaviour and host incarnating the CORBA objects are also mobile devices in nature.

Author: Mistry, Shailesh (200211016)
Title: Design of AHB-Wishbone bridge; ix, 47 p.; 2004.
Supervisor: Bhat, Amit
Call No.: 625.395MIS
Acc. No.: T00010
Keywords: AHB-Wishbone bridge; Circuitry; Wishbone architecture; Wishbone operation.
Abstract:

System-on-Chip (SoC) design is performed through integration of pre-designed components, called intellectual Property (IP). Design reuse is a critical feature in SoC design. Design reuse is the simple concept of using IP Cores of proven designs over again and again.

IP Cores may adhere to different interface standards. This leads to incompatibility between IP Cores. This requires the creation of custom glue logic to connect each of the cores together. A Bridge ensures that IP Cores can be reused with confidence in a multitude of systems supporting different bus protocols. Its purpose is to foster design reuse by alleviating System-on-Chip integration problems. This improves the portability and reliability of the IP Cores and system, and results in faster time-to-market for the end user.

The function of ARB-Wishbone Bridge is to map the control and address signals from one bus to another. The AMBA ARB is for high-performance, high clock frequency system modules. The ARB acts as the high-performance system backbone bus. ARB supports the efficient connection of processors, on-chip memories and off Chip external memory interfaces. The Wishbone System-on-Chip (SoC) Interconnection Architecture for IP Cores is a flexible design methodology for use with semiconductor IP cores.

Author: Modi, Bhavesh (200211041)
Title: A study of MPLS traffic engineering with constraint-based routing; viii, 50 p.; 2004.
Supervisor: Maitra, Anutosh

Call No:; 004.66MOD

Acc. No.: T00031

Keywords: Data transmission; MPLS Architecture; Multiplexing; Packet switching; Routing.

Abstract: Multi-protocol Label Switching (MPLS) is fast becoming popular for future communication networks running applications demanding high speed and Quality of Service. In this work, we have studied the evolution of MPLS, various issues related to MPLS and the architecture ofMPLS. The simplicity and functional capabilities ofMPLS enables various important applications over it such as Virtual Private Networks, Provisioning of Quality of Service and Traffic Engineering. The traffic engineering perspective of MPLS is studied in a greater detail as MPLS protocol has certain advantageous features in traffic engineering applications, the major being that it allows explicit routing, through which separately calculated routes can be specified for different traffic flows. The process of route calculation can be automated with the help of Constraint-based Routing. The thesis also presents a study on Constraint-based routing in MPLS environment. After that, a few classical constraint-based routing algorithms that consider bandwidth as constraint are investigated. The effectiveness of these algorithms is ascertained by means of simulation results. The concept of minimum interference routing and the corresponding algorithm MIRA is studied in greater detail in this work and presented in the thesis. The performance of MIRA was analyzed and factors that affect the performance were identified. Finally, the work suggests two modifications over MIRA based on the observations and analysis mentioned above. The primary philosophy behind the modifications are identifying the criticality of the resources and quantifying the order of the criticality. The performance of the suggested modified algorithms is benchmarked against classical MIRA algorithm and the simulation results are presented.

Author: Mythili, S. (200211039)

Title: Design and analysis of Anergy aware protocol- MPEARLE; 73 p.; 2004.

Supervisor: Ranjan, Prabhat

Call No.: 681.2 MYT

Acc. No.: T00030

Keywords: Energy aware protocol; Energy aware protocol—MPEARLE; MPEARLE; Routing protocols; Wireless sensor networks.

Abstract: Due to the technological advances and development in the field of micro electronic devices, the availability of compact, high-performance, customizable, intelligent devices at low cost has become reality. 'Wireless Sensor Network' (WSN) comprising such devices with customized sensors is used in monitoring the environment. The common demand of any application of WSN is the operation of the network for the guaranteed duration taking into account the limited battery capacity. The main consumer of battery power is the transceiver circuitry.

In WSN, the nodes form number of multi-hop routes of different hop count leading to the destination. Strategy for load balancing uses the cost metric calculated by the residual battery energy on nodes and transmission power for all nodes on the path. Dynamic transmitter power scaling is used to reach the neighbors with bare minimum power. The main focus of this thesis is on increasing the lifetime of the network through energy-aware routing protocol. This protocol borrows some ideas from Ad hoc On demand Distance Vector and Energy Aware, Load balancing protocol for Mars Sensor Network. Though this protocol is applicable for any wireless network of ad hoc nature, the 'lifetime' metric considered is primarily for Wireless Sensor Networks due to its deployment in hostile environment where human intervention is not possible. This work includes the design and simulation of the protocol named MPEARLE. Simulations are carried out on ns-2 [VINT] and results are discussed. A decent improvement in lifetime of sensor nodes as well as that of network, better uniformity in the node energy levels and reduction in packet loss is achieved in comparison to AODA.

Author: Nallagorla, V.S.R. Krishna (200211007)

Title: Automated Categorization of structured Documents; x, 54 p.; 2004.

Supervisor: Maitra, Anutosh

Call No.: 0005.72 NAL

Acc. No: T00004

Keywords: Categorization techniques; Document categorization; Naive Bayesian; Text categorization; TF-IDF; Term Frequency-Inverse Document Frequency.

Abstract: Automatic text categorization is a problem of assigning text documents to pre-defined categories. This requires extraction of useful features. In most of the applications, text document features are commonly represented by the term frequency and the inverted document frequency. In case of structured documents, dominant features are often characterized by a few sentences bearing additional importance. The features from more important sentences should be considered more than other features. Another issue in automated document categorization is the manageability and integrity of large volume of text data where the documents can be very large and often certain parts of the document misrepresent the primary focus of the document.

In this work, we study several document categorization techniques mostly in light of categorizing structured text. Categorization on summarized text is also studied in details with some specific purpose. While summarizing, the importance of appropriate sentences has been considered. The approach is verified by conducting experiments using news group data sets using three summarization methods. The set of whole documents and the summaries were subjected to a couple of classical categorization techniques, viz. Naive Bayesian and TF-IDF (Term Frequency-Inverse Document Frequency) algorithm. A major observation was preservation of the sanctity of the categorization even while that is based on the summary documents rather than the whole document. Goodness of the approach was verified on about 500 documents and the test results are enclosed.

Author: Oza, Hiral D. (200211037)

Title: Study and Development of Computer Aided Tool for Transceiver System Design; viii, 73 p.; 2004.

Supervisor: Gupta, Sanjeev

Call No.: 621.38418 OZA

Acc. No.: T00028

Keywords: Antennas; CAD (Computer Aided Tool); Radio receiving sets; Radio transmitters; Radio wave propagation; Transceiver; Transceiver system design.

Abstract: The aim of this thesis is to develop the GUI-based interactive software, which assists in designing transceiver for any modern communication system including GSM, CDMA, HIPERLAN, and WLAN. There are many trade-offs between transmitter and receiver parameters, and these need to be considered while designing the transceiver. Just like antenna, designing a transceiver system is difficult for the designer.

The antenna design and transmission line design tools are also incorporated in this software module. This software tool aims to aid transceiver/antenna designer by allowing the designer to know the effect of different parameters on the design of these subsystems. The CAD tool provides the graphical user interface.

The user-friendly software is developed using MATLAB®. The methods presented here considerably reduce the time and effort needed to write programs and does not require access to commercially available complex and costly design packages (like ADS, RF Workbench, SONNET, IE3D, etc).

The programs for this GUI-based interactive software tool were tested and validated by comparing output against that of commercial counterparts and also manually calculated and verified.

Author: Rahi, Sajajd S. (200211011)

Title: Design of architecture of artificial neural network; viii, 106 p.; 2004.

Supervisor: Chaudhary, Sanjay

Call No.: 006.32 RAH

Acc. No.: T00005

Keywords: Neural network—Architecture; Neural networks (Computer science); Soft computing.

Abstract: The objective of the work is to design and construct a model for creation of architecture of feed forward artificial neural network. The distributed genetic algorithms are used to design and construct the system. This thesis describes various encoding schemes suggested by researchers for the evolution of architecture of artificial neural network using genetic algorithm. This research proposes new encoding scheme called object based encoding for the evolution of architecture and also proposes data structures, genetic operators and repair algorithms for the system development. For evolution of weights during training, genetic algorithm is used. For evolution of weights, two dimensional variable length encoding scheme is proposed. For the same, two-point layer crossover and average crossover are proposed. The experiments are carried out on the developed system for the problems like 3-bit even parity. Which combination of genetic operators are more efficient for better design of artificial neural network architecture, is concluded by the experiments.

Author: Saksena, Nitin (200211018)

Title: Design and Implementation of a framework for Context aware mobile services; xii, 100 p.; 2004.

Supervisor: Srivastava, Sanjay

Call No.: 621.38456 SAK

Acc. No.: T00012

Keywords: Cellular telephone systems; Context aware mobile service; Framework for Context Aware Mobile Service; Mobile Service.

Abstract: Applications designed for mobile platforms are traditionally hampered by the limitations of the client devices, in particular limited user interface and the change of user environment due to mobility. Incorporating location of the device, and more generally the whole context of the user and device in the computation has clear advantages. A framework for context aware mobile services (FCAMS) targeted for cellular data network is proposed. We provide a detailed architecture of the framework. The design provides a generic way to add context to the mobile applications. An implementation of the framework along with an example service, ATM Finder is done. Functional analysis of the implementation is performed.

Author: Shah, Hardik K. (200211030)

Title: Design of frequency synthesizable delay locked loop; vii, 32 p.; 2004.

Supervisor: Bhatt, Amit

Call No.: 621.3815364SHA

Acc. No.: T00022

Keywords: Delay locked loop; Demodulator; Modulator; Phase locked loop; VLSI.

Abstract: As the speed performance of VLSI systems increases rapidly, more emphasis is placed on suppressing skew and jitter in the clocks. Phase-locked loops (PLLs) and delay-locked loops (DLLs) have been typically employed in microprocessors, memory interfaces, and communication IC's for the generation of on-chip clocks. But phase error of PLLs is accumulated and persists for a long time in a noisy environment, that of DLL's is not accumulated, and thus, the Clock generated from DLLs has lower jitter. Therefore, DLLs offer a good alternative to PLL's in cases where the reference clock comes from a low jitter source, although their usage is excluded in applications where frequency tracking is required, such as frequency synthesis and clock recovery from an input signal. Also, the DLLs adjust only phase, not frequency, so the operating frequency range is severely limited. Much work is done to improve the operating range of DLLs, but very less work is done to make DLLs frequency synthesizable. Here, frequency synthesizable DLL is implemented in simplest manner so that it can be useful with least complexity.

Author: Sharma, Ashish Kumar (200211017)

Title: Integrated Receiver Front-end: System Level Architectures and Design Issues for CDMA Based

Applications; xii, 86 p.; 2004.

Supervisor: Gupta, Sanjeev

Call No.: 621.3845 SHA

Acc. No.: T00011

Keywords: CDMA; CDMA based application; Integrated receiver; Radio frequency system; Receiver architecture.

Abstract: During the last decade, the world of mobile communications has experienced an enormous growth. Among the important factors has been possible by the migration from the original analog mobile phones to handsets using digital technology. Another important factor has been the rapid progress in silicon IC technology that made it possible to squeeze ever more digital functions onto a single chip. Since CDMA will be among the front running technologies for the mobile communication applications, the presented work uses its PCS mode air-interface specifications as the demonstration vehicle to highlight design issues involved with the system level receiver design.

This thesis deals with the design of integrated receiver front-end for CDMA-based mobile communication applications. Today circuits can be build in the mainstream CMOS technologies. For integration also it's a viable option since, the large digital back-end is exclusively done in CMOS, so an attractive option is to integrate the RF front-end in CMOS itself.

The work presented here outlines the design path of a receiver at system level, starting from fundamentals of RF design, architecture exploration, parameters responsible for degradation in receiver performance in this the focus is to study the effects of RF-Impairments on the QPSK modulation which is utilized in CDMA. Finally an analysis of CDMA receiver was done. The requirements of CDMA standard are mapped onto a set of measurable specifications for a highly integrated receiver. It is shown how a minimum required reception quality can be translated into specifications on the receiver's noise figure, image rejection, inter-modulation, etc. and how these specifications can be distributed among different blocks.

The simulation was carried out in MATLAB from Mathworks and ADS-2003 from Agilent technologies. The specifications for receiver components were taken from Maxim's Chipsets and related literature.

Author: Shenoy, Shakti Prasad (200211021)

Title: Space-Time Coding Techniques for Multiple Antenna Communications; viii, 4 p.; 2004.

Supervisor: Jadhav, Ashish

Call No.: 621.3824 SHE

Acc. No.: T00014

Keywords: Antennas—propagation; Mobile communication; Mobile communication system; MIMO; Multiple input multiple output; Space time coding techniques.

Abstract: Mobile communications has seen an explosive growth in the past decade. The reason for this growth can be traced to the increasing demand by the consumers for communication systems capable of exchanging information "anytime, anywhere" in the world. Rapid advances in semiconductor technology and signal processing techniques have led to the evolution of mobile communication devices from basic voice communication systems to those providing high quality data, image and multimedia services. One of the main requirements of next generation mobile communication standards therefore is provision for highly robust and reliable communication links for high data rate wireless services in a range of environments.

The presence of multiple scatterers in the mobile communication channel creates a multipath channel with time-varying fading characteristics. Traditionally, time and frequency diversity as well as spatial diversity techniques at the receiver have been used to combat the effect of multipath propagation. Recent research in channel coding over the less-studied transmit diversity techniques have led to a new class of channel codes for spatial diversity systems called space-time codes that exploit the multipath nature of the channel to provide enhanced link stability. Moreover these codes promise a phenomenal increase in throughput of the channel by using multiple antennas at the transmitter and the receiver. In this thesis we study the theory and practice of

space-time coding techniques for multiple antenna communication systems. We discuss the information theoretic aspects of the so-called Multiple-Input-Multiple-Output (MIMO) channels and examine the various methods adopted for the design of space-time codes over such channels and their relative merits. We also carry out simulation to validate the claim that space-time codes can provide significant increase in SNR in multipath fading channels.

Author: Srinu Babu, G. (200211033)
Title: Voronoi Diagram Modelling for wireless Ad-hoc Sensor network coverage; vii, 40 p. 2004.
Supervisor: Sinha, V. P.
Call No.: 681.2 BAB
Acc, No.: T00024
Keywords: Voronoi diagram modelling; Wireless Ad-Hoc sensor networks; Wireless sensor networks.
Abstract: This thesis aims at a basic geometrical understanding of Voronoi diagrams and Voronoi diagram modelling for Wireless Ad hoc Sensor coverage. What is known as the Fortune algorithm for constructing Voronoi diagrams is explained. Implementation of the Fortune algorithm is also shown as a part of this thesis. Several applications of Voronoi diagrams are explained with practical examples.

Coverage problem in wireless ad hoc sensor networks is modelled with Voronoi diagram and its dual Delaunay triangulation. The problem of best and worst coverage for a wireless ad hoc sensor networks are discussed. Coverage paths like Best and worst paths are explained in detail. The algorithms for determining best coverage paths and worst coverage paths are described and implemented in MATLAB& C.

Results for best coverage paths and worst coverage paths are shown for a given number of sensors placed in the sensor field.

Author: Tandon, Dheeraj (200211022)
Title: Convert Communication in TCP/IP Network; ix, 73 p.; 2004.
Supervisor: Mitra, Suman K. and Mathuria, Anish
Call No.: 004.62 TAN
Acc. No.: T00015
Keywords: Covert communication; Internet protocol; Protocol suite; Socket interface; TCP/IP (programming); Transmission control protocol.
Abstract: This thesis explores the area of Covert Communication in TCP/IP network (Internet). We investigate various protocols of TCP/IP suite, which have potential to be used for covert communication on the network. In this thesis we propose methods for covert communication using Internet protocols that are otherwise intended for transmission of control information. The methods use IP spoofing concept with ICMP or DNS query messages. The existence of these covert channels is known but exploitation of these in concrete methods for covert communication is the contribution of this work. The proposed methods are more efficient in the amount of data that are hidden per IP packet as compared to several existing methods on packet manipulation. The important thing is that whatever method is used for covert communication it should not hinder the normal communication on the network then only undetectability of these covert channels would be ensured. So no changes in protocol structure, router configuration etc would be required for the working of these methods for covert communication. For the same reason in our proposed methods we keep this thing in mind. That's why except at sender and receiver no new software is needed to implement the methods.

Author: Thacker, Grishma D. (200211036)
Title: Technique to Improve Revocation Mechanism and Enhancement of CA's Services; iv, 54 p.; 2004.
Supervisor: Jadhav, Ashish

Call No.: 005.82 THA

Acc. No.: T00027

Keywords: Certificate revocation list; Certification authority (CR); Cryptography; Public key infrastructure; Publics key cryptography.

Abstract: Public Key Cryptography [PKC] is becoming popular in the world of security because of its promising features like authentication and non-repudiation along with integrity and data confidentiality. It has been possible to achieve an electronic equivalent of hand written signatures that are considered to be the most common method of providing identity proof in a non-electronic world, thanks to PKC techniques. Public Key Infrastructure [PKI] is a technology that supports PKC to achieve its intended services by implementing PKC concepts. It is considered to be one of the potential technologies for the future of e-business and e-governance. Digital certificates are one of the most important components of PKI. They are issued and signed by a trusted third party named Certification Authority to provide trust worthy binding between the entity and its public key, thus, they impute trust in the public key of a claimant. The certificate has predefined validity period after which they expire. But sometimes during its valid lifetime due to certain events, the certificate doesn't remain valid. A need arises to declare its invalidity implying withdrawal of trust that was imputed in it at the time of issuance. This event is called 'revocation' of the certificate. The information regarding this event of revocation has to propagate to the entire community that might use the certificate in question for its important transaction. 'Certificate Revocation' is one of the key issues in PKI because security of any transaction relies on the validity of the certificate used in it. Hence, the status of these certificates in terms of 'valid' / 'non- valid' becomes important information to be processed, conveyed, acquired, and managed securely. There are many mechanisms proposed for the certificate revocation information distribution.

My primary concern is to focus on some of these mechanisms and to provide some solution for this problem. I've proposed a method named "Staggered CRLs". It uses delta CRLs and shows how a CA can avoid generation of signature over the voluminous CRL and still can provide more timely information than the traditional CRL. CRLs are issued along with delta CRLs with 'slight' modification. The method avoids prefixing of next update time of CRL and makes it dynamic based on some other criteria. It provides more timely information at lesser frequency of CRL. My second proposal is about how a CA can enhance its services to the user community. I suggest to go beyond merely providing revocation information about the certificate and to add more value to the CA services by providing further information about the certificates.

Author: Thakar, Lalitkrushna Jagdishchandra (200211012)

Title: Chaotic communication system for IEEE 802.11b (WLAN); xi, 46p.; 2004.

Supervisor: Chakka, Vijaykumar

Call No.: 621.38212 THA

Acc. No.: T00006

Keywords: Chaotic communication systems; Communication protocols; Communication standards; IEEE 802.11B; Wireless local area network; WLAN communication systems.

Abstract: Today's WLAN (IEEE 802.11b) is most attractive solution for wireless data communication at higher rate. Chaotic signals, by virtue of their wideband characteristic, are natural candidates for wideband communication environment. The use of chaotic signals in communication thus naturally inhabits the advantages offered by conventional spread spectrum communication system.

A novel Chaotic Code Division Multiple Access (CCDMA) scheme is proposed for IEEE 802.11b Physical layer implementation based Direct Spread Spectrum Technique. The work carried out in this thesis consists of investigation of efficient chaos based architecture for IEEE802.11b (WLAN) to support more number of users. Characteristic of various chaotic signal are studied, results in robust multi user chaotic systems, which are characterized by sensitive dependence on initial conditions, random noise like behaviour, and continuous broadband power spectrum. The properties of chaotic signals comprise the requirements for the signals applied in broadband communication systems, particular for spread-spectrum, multi-user and secure communications.

Simulation results of proposed model open up a new improved architecture with effective Bit error rate performance in multiuser. This simulation is done in A WGN environment. The simulation is

carried out as per the specification of IEEE 802.11b standard.

Author: Trivedi, Jigish S. (200211013)
Title: A hybrid approach to speech recognition in multi-speaker environment; viii, 43 p.; 2004
Supervisor: Kudchadkar, Arvind P.
Call No.: 006.454 TRI
Acc. No.: T00007
Keywords: Speech recognition; Speech recognition, multi-speaker environment.
Abstract:

Recognition of voice, in a multi-speaker environment involves speech separation, speech feature extraction and speech feature matching. Traditionally, Vector Quantization is one of the algorithms used for speaker recognition. However, the effectiveness of this approach is not well appreciated in case of noisy or multi-speaker environment. This thesis describes a thorough study of the speech separation and speaker recognition process and a couple of benchmark algorithms have been analysed. Usage of Independent Component Analysis (ICA) in speech separation process has been studied in minute details. The accuracy of the traditional techniques was tested by simulation in MATLAB. Later, a hybrid approach for speech separation and speaker recognition in a multi-speaker environment has been proposed. Test results of a series of experiments that attempt to improve speaker recognition accuracy for multi-speaker environment by using the proposed hybrid approach are presented. Speaker recognition results obtained by this approach are also compared with the results obtained using a more conventional direct approach and the usefulness of the hybrid approach is established.

Author: Vichare, Chirag Vishwas (200211031)
Title: Speech enhancement using microphone array for hands-free speech applications; ix, 31p.; 2004.
Supervisor: Chakka, Vijaykumar
Call No.: 621.384133 VIC
Acc. No.: T00023
Keywords: Microphone array; Microphone Radio engineering; Speech enhancement; Speech processing system; Speech synthesis.
Abstract:

This thesis addresses the problem of multi-microphone speech enhancement using GSVD (Generalized singular value decomposition) based optimal filtering algorithm. This algorithm does not require any sensitive geometric information about the array layout, hence is more robust to deviations from the assumed signal model (e.g. look direction error, microphone mismatch, speech detection errors) as compared to conventional multi-microphone noise reduction techniques such as beamforming. However, high computational complexity of this algorithm makes it unsuitable for practical implementation.

The work presented in this thesis discusses a recursive version of this algorithm in which GSVD of the data and noise matrices at any instant are updated using GSVD of the matrices available at previous instant as new data arrives in. It is shown that this recursive GSVD updating scheme reduces the computational complexity of this algorithm drastically making it amenable to practical implementation. Various issues related to its implementation are addressed.

This thesis also explores the possibility of further reduction in computational complexity, by incorporating GSVD based optimal filtering algorithm in Generalized Side lobe Canceller (GSC) type structure in detail without causing any performance degradation in terms of background noise reduction and speech quality.

Author: Vipperla, Ravi Chander (200211014)
Title: Incorporation of mobility model of nodes in zone routing protocol for mobile Ad-hoc wireless networks; viii, 48 p.; 2004.
Supervisor: Chakka, Vijaykumar

Call No.: 004.65 CHA

Acc. No.: T00008

Keywords: Ad-hoc wireless networks; Computer network architectures; Mobile Ah-hoc networks; Routing protocol; Wireless communication systems.

Abstract:

Ad Hoc wireless networks are characterized by dynamically changing network topology due to relative motion of the nodes. This leads to the exchange of large number of control packets between the nodes to maintain the network topology resulting in reduced throughput in such networks and wastage of bandwidth in the exchange overhead control packets.

In this thesis, we propose the use of mobility models of the nodes to improve routing protocol performances. The basic idea is that the neighboring nodes exchange their mobility models (i.e., location and velocity information) during network updates and use this information to determine more stable routes that do not become invalid due to the nodes movement. This technique has been incorporated into one of the popular routing protocol for Mobile Ad Hoc Networks known as the 'Zone Routing Protocol'.

Among envisaged improvements with the above technique is determination of stable routes leading to reduction in the number of route failures, reduction in the number of overhead control packets, Scope for the use of directional antennas, bandwidth efficiency and reduction in power consumption at mobile nodes.

Simulations have been performed in MATLAB to analyse the performance of the ZRP with mobility models incorporated and the analysis results show decent improvements.

Author: Agrawal, Awkash (200311017)
Title: WebLab : A Framework for Remote Laboratories; vii, 77 p.; 2005.
Supervisor: Srivastava, Sanjay
Call No.: 004.678 AGR
Acc. No.: T00043
Keywords: Internet; World Wide Web.
Abstract: Remote laboratories have been proposed and implemented in the past to address a number of issues, namely wider access to high-end expensive experiments, safety, and better resource utilization. However, the existing projects are designed for specific knowledge domains, and normally run in a dedicated access mode. There is a pressing need to share the limited laboratory resources of the academic institutions in India among the universities. Studies have suggested that most of the Indian universities have basic computing and Internet facility. In this work we propose a web-based 3-tier architecture (WebLab) that provides shared batch mode access to the experiments over low-bandwidth network to maximize the laboratory utilization. A generic experiment is modeled as a set of inputs, outputs, and constraints. A lab/experiment registration toolkit is designed to capture the metadata for the labs and experiments. This allows for a rapid and standardized integration of the experiments with the WebLab. A proof of concept lab is implemented on this architecture.

Author: Bala, Shashi (200311024)
Title: Shorted Microstrip Patch Antenna; 53 p.; 2005.
Supervisor: Gupta, Sanjeev
Call No.: 621.3824 BAL
Acc. No.: T00048
Keywords: Microstrip antennas; Microstrip patch antenna; Microwave antennas; Strip transmission lines.
Abstract: In this thesis, electrically small microstrip patches incorporating shorting posts are thoroughly investigated. These antennas are suitable for mobile communications handsets where limited antenna size is a premium. In particular, it is shown that the zero mode of the unloaded MSA (Microstrip Antenna) plays a central role for reducing the lowest operation frequency of the loaded MSA. The studies carried out allow the determination of all relevant antenna parameters for different post specifications and can easily be extended for different patch architectures.

Author: Bhandari, Kunal (200311016)
Title: A Hybrid Approach to Digital Image Watermarking using Singular Value Decomposition and Spread Spectrum; vii, 47 p.; 2005.
Supervisor: Jadhav, Ashish
Call No.: 005.8 BHA
Acc. No.: T00042
Keyword: Data security; Digital watermarking; Watermarking algorithm.
Abstract: We have seen an explosive growth in digitization of multimedia (image, audio and video) content and data exchange in the Internet. Consequently, digital data owners are able to massively transfer multimedia documents across the Internet. This leads to wide interest in security and copyright protection of multimedia documents. Watermarking technology has evolved during the last few years to ensure the authenticity of multimedia content. We compare the widely used spread spectrum technique with the newly evolved technique based on Singular Value Decomposition (SVD) for watermarking digital images. The techniques are tested for a variety of attacks and the simulation results show that the watermarks generated by both the techniques have complimentary robustness properties. We propose a new hybrid technique for watermarking digital images, combining both paradigms, which is capable of surviving an extremely wide range of attacks. Our technique first embeds a watermark in an image using spread spectrum concepts and then to increase the robustness, another SVD based watermark is added such that they do not interfere with each other. Our technique is robust against a wide range of distortions like filtering, noise adding, lossy compression, print & rescan and non-linear deformations of the signal

such as, histogram manipulation, dithering and gamma correction. The watermark added by our technique is perceptually invisible. The effectiveness of this technique is demonstrated against a variety of standard image processing attacks.

Author: Bhatt, Krutarth (200311038)
Title: Multiple Watermarking Schemes for Copyright protection; x, 77 p.; 2005.
Supervisor: Mitra, Suman K.
Call No.: 005.8 BHA
Acc. No.: T00057
Keywords: Copyright; Digital watermarking; Watermarking techniques.
Abstract:

Recent advances in digital communication and storage technologies have brought major changes for consumers. High capacity hard disks and DVDs can store a huge amount of audiovisual data. In addition, faster Internet connection speeds and emerging high bit rate DSL connection provide sufficient bandwidth for entertainment networks. These improvements in computer networks and communication technology are changing the economies of intellectual property reproduction and distribution. Intellectual property owners must exploit the new ways reproducing, distributing, and marketing their intellectual property. However a major problem with current digital distribution is the great threat of piracy. Digital watermarking is proposed as a solution to avoid digital piracy.

In this work we have addressed multiple watermarking to increase robustness requirement for copyright protection and ownership prevention. Taking into account the scenarios for the present content distribution environment, we do rely on sending and distributing the content through physical channels along with digital network communication and distribution. We may publish the content in some newspapers and/or magazines etc. According to our belief there are very few techniques that are highly robust against unintentional image processing like print-scan, dithering that are routinely performed during publication of an image along with the conventional attacks that are performed on digital representation of an image. We have developed two techniques; one is "Multiple Watermarking using feature selection" and the other is "Multiple Watermarking in Hybrid SVD-DCT domain". Both the techniques are highly robust against various attacks including JPEG-Lossy compression, Blurring, Median filtering, Rotation, Cropping, Scaling, Rescaling, Histogram Equalization, Intensity Adjustment, Gamma Correction, Gaussian Noise Addition, Salt & Pepper Noise Addition, Uniform Noise Addition, Dithering, Print & Rescan, Intentional Tampering, Pixelate etc. Imperceptibility, Security and Reliability of Detection are also satisfied by the proposed techniques.

Author: Chandra Mouli, P. (200311009)
Title: Acoustic Source Localization Using Audio and Video Sensors; xi, 45 p.; 2005.
Supervisor: Chakka, Vijaykumar
Call No.: 621.3828 MOU
Acc. No.: T00036
Keywords: Acoustical communication; Acoustical engineering; Acoustical source; Acoustic source localization; Audio sensors; Sensors; Video sensors.
Abstract:

Problem of localizing an acoustic source using microphone array and video camera is studied. In general, it's quite obvious that a human with both, eyes and ears can make out things more accurately than to a human who is either blind or deaf. We have taken a position that a machine like man can do better in localizing an object if relies both on audio and video sensors. For localization using microphone array, Time Delay Estimate (TDE) based localization schemes are used. The TDE based localizers are fast enough to give the results in real time. Generalized Cross Correlation along with Phase Transform is used for finding the time delay of arrival at a microphone array. With these time delay of arrivals and known array geometry, spherical equations are written and these equations are solved using Least squares estimation to get the position of the source. To get the video cue, we tried to localize the human face/body in a given image/video. A clustering property of human skin in YCbCr color space is exploited to do this task. A skin color model is built from a large set of image-database to segment out the human skin from the image. The database is collected so that the same model works for different colors of skin (white, black and yellow). Nearly one crore pixels (twenty five lacks for skin pixel and seventy of five lacks for non-skin pixels) of twenty different people under different illumination conditions

are considered for modelling of skin color and non-skin color histograms. Once the face location in the image is found out, a lookup table method is discussed using which one can convert the given pixel number to a location in the room with respect to camera coordinates for fixed distances. Now both the audio and video estimates are fused together to give a better estimate. It is shown in this thesis that, taking the video cues along with the audio cues improves the estimate. The developed localizer can give two estimates of the source in one second.

Author: Changela, Jasankumar R. (200311035)
Title: Performance Analysis of Fair Schedulers under Heterogeneous Traffic; ix, 67 p.; 2005.
Supervisor: Jotwani, N. D.
Call No.: 621.38216 CHA
Acc. No.: T00055
Keywords: Data transmission system; Packet switching (Data transmission); Switching methods.
Abstract:

In this thesis, the role of the packet scheduling discipline has been studied in providing QoS over the Internet. The fairness and scalability requirements expected to be satisfied by the scheduling discipline have been analysed, with reference to the two categories under which schedulers are broadly classified: Round-robin-based schedulers and Timestamp-based schedulers. In particular, the basic principles and design goals of three specific Fair Schedulers WDRR, NestedDRR and StratifiedRR have been studied.

The Network Simulator (ns-2) tool has been enhanced to support WDRR, NestedDRR and StratifiedRR schedulers. To analyse the performance of WDRR, NestedDRR and StratifiedRR under MPEG, CBR and BE traffic, simulations have been carried out for specific load conditions under single hop and two hop topologies. From simulation results it has been observed that, as its reserved rate increases, MPEG traffic achieves better performance under StratifiedRR. Also, degradation in the performance received by other contending traffics is greater under StratifiedRR. It has been identified that, for fixed value of Load Factor, as quantum increases, the End-to-End delay and End-to-End delay-jitter of MPEG traffic under WDRR show greater variation than that seen under NestedDRR. Based on these results, an improvement over StratifiedRR has been proposed which is expected to make the delay and delay-jitter seen by a flow independent of the packet sizes in other flows.

Author: Desai, Bhumi (200311033)
Title: Dual-Band Microstrip Antenna Design; 48 p.; 2005.
Supervisor: Gupta, Sanjeev
Call No.: 621.3824 DES
Acc. No.: T00053
Keywords: Microstrip antennas; Microstrip antennas—Design; Microwave antennas; Strip transmission lines.
Abstract: Multi-frequency microstrip antennas are very much in demand due to their physical and mechanical properties like small size, lightweight, thin profile, low power consumption, and ease of implementation in the domestic applications. Some designs of dual-band microstrip patch suitable for GSM 900/1800 base station operation are already a research topic. Dual frequency microstrip antennas are also used in GPS and SAR. Commercially, these are deployed in RFID tags. But for the antenna to be useful in all these applications, its behavior like return loss, bandwidth, beam width, radiated power, gain, and directivity, at both the frequencies, should be nearly identical. The purpose of this work is to design the microstrip patch for dual frequencies of 945 MHz and 1960 MHz. Two new approaches called Coplanar patches and Overlapped patches are proposed. Then some of the existing techniques like Stacked patches, Dual slot loaded patches and Dual frequency PIFA are explored for our design specifications. Finally, the comparison of all the design aspects including the proposed ones is carried out in this work.

Author: Gandhi, Ratnik (200311005)
Title: Selfish Routing and Network Creation Games; vi, 45 p.; 2005.
Supervisor: Chatterji, Samaresh
Call No.: 621.3821 GAN
Acc. No.: T00034

Keywords: Network games; Routers (Computer networks); Routing (Communications).

Abstract: This work studies the two important problems of routing and network creation in the situation of selfish behavior of agents. In routing, agents want to send their data from source to destination. They try to reduce cost incurred in the process of routing. In network creation, agents create agent-to-agent link to form a network on which they can Communicate. Here there are two types of cost incurred: link creation cost and routing cost. Each agent tries to reduce his own cost. To study degradation caused by selfish behavior of agents we primarily use the standard notation of Price of Anarchy, which is ratio of the cost incurred at Nash equilibrium to the optimal cost. We show some results on Price of Anarchy and on different cost functions for above two problems, we propose a new model in network creation and show a polynomial time algorithm to verify Nash equilibrium.

Author: Garg, Nitin (200311007)
Title: Performance Analysis of JDO in J2EE Architecture; xi, 72 p.; 2005.
Supervisor: Chaudhary, Sanjay
Call No.: 005.133 GAR
Acc. No.: T00035
Keywords: JDO (Java Data Object); J2EE (Computer programming language); Computer programming languages.

Abstract: Data persistence is one of the most important aspects of any enterprise wide application. An enterprise data persistence solution must provide speedy client transactions, ensure data integrity over time, and be able to persist data through such everyday catastrophes as system crashes and network failures. Object-oriented applications that use the Java 2 Enterprise Environment (J2EE) have a variety of persistence technologies at hand. Two prominent ones among these are entity beans and recently introduced Java Data Objects (JDO). Entity beans provide a robust container-based persistence framework attributed with various middleware services. However, over the years the use of entity beans has brought into light a number of its drawbacks. Component level inheritance and dynamic querying are not supported appropriately, and the whole approach seems to be overweight. In order to overcome these weaknesses, researchers proposed a JCA-compliant resource adapter, which allows the use of Java Data Objects (JDO) instead of entity beans and introduces a lightweight, easy to use and powerful transparent persistence layer for the Java 2 Enterprise Environment. We have presented a detailed analysis of JDO technology and compared its performance with contemporary technologies. Analysis is done to compare the response time, execution time; maximum tests per second as number of concurrent clients increases of various object persisting techniques.

Author: Gupta, Dharmendra (200311010)
Title: Routing and Wavelength Assignment in DWDM Networks; vii, 109 p.; 2005.
Supervisor: Roy, Anil K.
Call No.: 621.3821 GUP
Acc. No.: T00037
Keywords: DWDM (Dense Wavelength Division Multiplexing); Wavelength Division Multiplexing; Optical communications; Optical networks.

Abstract: All-Optical Networks employing Dense Wavelength Division Multiplexing (DWDM) are believed to be the next generation networks that can meet the ever-increasing demand for bandwidth of the end users. The problem of Routing and Wavelength Assignment (RWA) has been receiving a lot of attention recently due to its application to optical networks. Optimal Routing and Wavelength Assignment can significantly increase the efficiency of wavelength-routed all-optical networks. This thesis presents some new heuristics for wavelength assignment and converter placement in mesh topologies. Our heuristics try to assign the wavelengths in an efficient manner those results in very low blocking probability. We propose novel static and dynamic assignment schemes that outperform past assignment schemes reported in the literature, even when converters are used. The proposed on-line scheme called Round-Robin assignment outperforms previously proposed strategies such as first-fit and random assignment schemes. The performance improvement obtained with the proposed static assignments is very significant when compared with the dynamic schemes. We designed and developed a simulator in Matlab6.5 that supports the 2D mesh topology with DWDM as well as random topology generation. We ran extensive simulations and compared our heuristics with those reported in the literature. We have examined converter

placement in mesh topologies and proposed that placing converters at the center yields better results than uniform placement when dimension order routing is employed. We introduced a new concept called wavelength assignment with second trial that results in extremely low blocking probabilities when compared to schemes based on a single trial. Our proposed schemes are simple to implement and do not add to the cost. Thus we conclude that wavelength assignment plays more significant role in affecting the blocking probability than wavelength converters. The algorithm yields significant improvements in terms of the request blocking probability over traditional techniques. Also we have observed from simulated results that by using even limited conversion of degree two is sufficient to achieve performance of full conversion. We have achieved this performance by using our better heuristic technique of establishing light paths.

Author: Jain, Abhay (200311019)
Title: Protecting Structures on Heap from Buffer Overflow Vulnerabilities with TIED–LibsafePlus; ix, 83 p.; 2005.
Supervisor: Mathuria, Anish
Call No.: 005.8 JAI
Acc. No.: T00045
Keywords: Computer security; TIED-LibsafePlus.
Abstract:

In spite of the numerous defenses that have been devised to combat the buffer overflow attack, buffer overflow vulnerability in the C programs still exist as the one widely exploited by the attackers to subsume the privileges of host on remote machine. This is subsequently used to launch even more precarious attacks. A buffer is said to be overrun if data is copied beyond its bounds thus overwriting the memory locations adjacent to the buffer. Buffer overflow vulnerabilities occur primarily due to two reasons. One is the absence of automatic bounds checking of arrays and pointer references in the language and other being the use of unsafe C library functions that don't range check the buffers before copying data into them.

This thesis proposes a defense mechanism for preventing heap buffer overflow. It is built over another solution to buffer overflow problem called TIED-LibsafePlus. TIED-LibsafePlus extracts the type information of all the buffers (except the one lying on heap) from the raw debug information present in the binary and rewrites it into the binary as new specific tables that are accessed by the library to find the size of buffers before copying the data into them by intercepting the unsafe C library functions. TIED-LibsafePlus cannot prevent the overflow of the buffers that are allocated on heap as member of some user defined data type like C structure. A manually crafted attack is demonstrated that changes the flow of control by overflowing such buffers. To prevent these buffers from getting overrun using the approach employed by TIED-LibsafePlus, it is necessary to dynamically find out the type of the structure allocated on heap, which is not feasible with the current implementation of malloc family of functions. Thus to achieve this the proposed solution augments the binary with some more type information pertaining to structures defined in the program, which is then accessed by the safe library. This thesis describes how the structures allocated on heap can be protected from buffer overflow at the cost of this extra type-information and extra checking performed by the library at run time.

Author: Jain, Alok (200311002)
Title: Performance of MIMO in Correlated Rayleigh Flat Fading Channels; vii, 49p.; 2005.
Supervisor: Jadhav, Ashish
Call No.: 621.384135 JAI
Acc. No.: T00033
Keywords: Antenna; Communication system; MIMO Communication system; MIMO (Multiple Input Multiple Output); OFDM.
Abstract:

The recent interest in Multiple Input Multiple Output (MIMO) communication systems was initiated by the theoretical work of Telatar. The development in the field of random matrix theory is the basis of these studies. The assumption in the mathematical model for studying MIMO turned out to be too idealistic for realistic (correlated) channel condition. This lead to an exaggeration of performance of MIMO.

This thesis deals with quantification of performance of MIMO in realistic channel conditions with

the emphasis on study of working of MIMO receivers. Our definition of MIMO contains both diversity systems and spatial multiplexing systems.

For the simulation of realistic channel conditions a correlated fading channel model with lack of rich scattering is used. To perform simulations for N transmit and M receive MIMO systems there is a need for having N x M correlated fading envelops. We propose a novel and simplified technique to extend the algorithm for two correlated fading envelops given by Richard and Jeffery.

Various analytical studies on the effect of correlated multi-path channel on performance of spatial multiplexing have been done. These studies focus on capacity cumulative distribution function. Effect of various degree of correlation on other performance measures like diversity gain and error probability have been not done. This is due to lack of simple method of generation of correlated Rayleigh fading envelops. By making use of the extended algorithm we have been successful in carrying out simulation to observe the effects on the performance.

Recently there is interest in extending the concept of MIMO in wireless communication for sensor networks. The motivation behind it is energy efficiency of sensor nodes. Our results have implications on this venture.

Author: Jain, Rajul (200311036)
Title: Contributions to Parasitic Computing; vii, 54p. 2005.
Supervisor: Mathuria, Anish
Call No.: 005.8 JAI
Acc. No.: T00056
Keywords: Computer security; Data security; Parasitic computing.
Abstract:

Internet is a huge connection of networks. To ensure reliable communication on the Internet a layered architecture is used, with various protocols functional at each layer. The way these protocols are used on the Internet, it is possible to exploit them to do computations covertly. This kind of computing is known as Parasitic Computing. Parasitic computing is a kind of covert exploitation in which the parasite hides the computation in standard communication protocol and sends it to target(s), who unwillingly produce the output of the hidden computation as part of the communication session.

We show that Internet checksum based parasitic computing can be used to solve three well-known problems, Discrete Fourier Transform, Matrix multiplication and Pattern matching. We describe how CRC checksum can be used to do primality testing using parasitic computing.

A more efficient implementation of Internet checksum based parasitic computing is proposed and simulated. A comparison based on false negatives with the existing implementation is given. Results show that the proposed scheme performs better in terms of the selected parameter of false negatives. However, there is additional communication overhead associated with it.

Parasitic computing can be applied in the field of security protocols. A novel sorting algorithm, Ker-sort is devised by exploiting ticket lifetimes in Kerberos and tested on Kerberos version 5.0. Run time analysis of the algorithm is given, and a comparison with existing distributed sorting algorithms is also presented. Brute-force cryptanalysis involves doing an exhaustive search in the key space. Using parasitic computing the parasite can offload the encryption or decryption operations involved in doing exhaustive search to the target(s). A theoretical cryptanalysis of SKIP and IP authentication header protocols using distributed exhaustive search is proposed.

Author: Kabra, Mukul (200311034)
Title: Performance Evaluation of OFDM Technique for High Speed Communication Applications; xi, 98 p. 2005.
Supervisor: Maskara, S. L.
Call No.: 621.3821 KAB
Acc. No.: T00054
Keywords: Communication network; High speed communication; OFDM.
Abstract:

The Internet revolution has created the need for wireless technologies that can deliver data at high speeds in a spectrally efficient manner. However, supporting such high data rates with

sufficient robustness to radio channel impairments requires careful selection of modulation techniques. The demand for high-speed mobile wireless communications is rapidly growing. OFDM technology promises to be a key technique for achieving the high data capacity and spectral efficiency requirements for wireless communication systems of the near future.

Orthogonal frequency division multiplexing (OFDM) is a special case of multi-carrier transmission, where a single data stream is transmitted over a number of lower rate sub-carriers. OFDM is currently being used in Europe for digital audio and video broadcasting. The IEEE standardization group decided to select OFDM as the basis for their new 5-GHz standard, targeting a range of data stream from 6 up to 54 Mbps. This standard was the first one to use OFDM in packet-based communications, while the use of OFDM until now was limited to continuous transmission systems. OFDM is also being considered as a serious candidate for fourth generation cellular systems. In this project, transmitter, channel and receiver were simulated with various parameters, to evaluate the performance and different possibilities in the implementation. Also, some considerations about forward error correction coding, interleaving, synchronization and channel estimation are given to improve the system performance.

Author: Khera, Neha (200311041)
Title: Design of Laser Driver Circuit; viii, 30 p.; 2005.
Supervisor: Roy, Anil K. and Parikh, Chetan D.
Call No.: 621.38152 KHE
Acc. No.: T00060
Keywords: Integrated circuits; Optoelectronic devices; Optoelectronic Integrated Circuit (OEIC); Optoelectronics; Semiconductors.

Abstract:

Designing an Optoelectronic Integrated Circuit (OEIC) is an attractive field of research as it bridges the interface between electrical and optical components. The design of laser driver in optical transmitter is very critical because it requires large output current and high speed. To date, majority of laser drivers have been designed using Bipolar Junction Transistor (BJT) due to wider bandwidth and good quality of passive components. However, the standard digital Complementary Metal Oxide Semiconductor (CMOS) technology provides advantages, such as, low power, low cost of fabrication due to high production yield, and a higher degree of integration. Thus, the silicon CMOS technology, which is well known for low cost and high density, is preferred to design an Optoelectronic circuitry.

Under this thesis, the work undertaken pertains to devising cascode-based laser driver circuit operating at 2.5 Gbps, using Hewlett Packard CMOS26G 0.8mm CMOS process. The devised circuit integrates well with the 1550nm rate equation based equivalent circuit model generated from R-soft design tool kit OptSim 3.6. This is definitely a step forward on the existing topologies, which have worked on 850nm VCSEL. The thesis projects reduction in number of transistors and, consequently, the chip area occupied by the driver. In nutshell, what has been done on this score and what remains to be done has been explained in detail in chapter-4 of the thesis under the title "conclusion & future scope".

Author: Kishore, G. Pavan Krishna (200311006)
Title: A Novel Local Oscillator Circuit for Sub-Harmonic Mixer; ix, 58 p.; 2005.
Supervisor: Biswas, R. N. snd Parikh, Chetan D.
Call No.: 621.381 533 KIS
Acc. No. T00062
Keywords: Cellular telephone systems; Communication systems; Electric; Microwave; Oscillators; Oscillators circuits; Wireless communication.

Abstract:

Direct Conversion RF transceiver is the enabling technique for the next generation cellular and personal communication devices striving for miniaturization, long life of battery and cost effectiveness. Existing techniques of Direct Conversion suffer from undesired carrier radiation from the receiver. This leads to distortion in the signal received by the users in the close proximity. The proposed transceiver design is an approach to address the discussed issue of carrier radiation. The existing systems use Sub Harmonic mixer to overcome this problem with a sinusoidal Local Oscillator (LO) running at half of the required carrier frequency. The W-CDMA systems which use

QPSK modulation need eight phases of the LO, the generation of which consume large power due to the linear circuits used. The proposed design implements the octet phase LO using non-linear circuits. This leads to the significant improvement in terms of power consumption and area. The core work of the thesis involves designing and analysis of new circuit topology that uses CMOS inverter chain for generating the octet-phase trapezoidal LO, to drive the Sub Harmonic mixer. The improvements are possible through the reduced size of transistors used in inverter and its non-linear operation. Thorough analysis of the circuit is performed for both sinusoidal and trapezoidal LO. Competitive results are obtained from the analysis of the design in terms of conversion gain, carrier suppression and Input referred 3rd order Intercept Point (IIP3). The design is modified to make it robust for varying ambient temperatures using a junction diode. A two port model of the Sub Harmonic mixer is derived, which proves a non-sinusoidal LO can be used in place of sinusoidal.

Author: Kumara, Pooja (200311012)
Title: ACIDS: Automated Co-stimulation based Intrusion detection System with a sense of Dynamic Self; viii, 79 p.; 2005.
Supervisor: Mathuria, Anish
Call No.: 005.8 KAM
Acc. No.: T00039
Keywords: Intrusion detection system; Computer networks-security measures.
Abstract:

Automated Co-stimulation based Intrusion detection system with a sense of Dynamic Self, or ACIDS, is a distributed architecture for intrusion detection systems. Other than the already used aspects of human immune systems like negative selection, clonal selection, gene expression etc., the novelty of ACIDS is that it incorporates two features of the human system not used previously, namely thymus and vaccination.

Self is defined as the set of normal connections observed on the network. All the existing systems are modeling the self as a static entity, when it should have been otherwise. Also, human immune system needs two disparate signals before taking some action against the antigen. The first signal is generated at the point of attack and stimulates the immune system for rigorous detection. The second signal is known as co-stimulation, and it stimulates the immune system for taking the action against an antigen. All the existing artificial immune models are also seeking co-stimulation, but it is generated through human intervention. This makes them unusable in real time. Another drawback in the existing systems is that they start from the scratch, i.e. they do not derive knowledge from the existing data of the intrusions.

ACIDS aims to overcome the above drawbacks of existing models. It includes a module called thymus that dynamically updates the self's definition of the system. To best of our knowledge, this concept is being used for the first time in intrusion detection systems. In CIDS, hosts are monitored at two levels, network level and operating system level. Whenever an anomaly is detected at the network level, ACIDS monitors the activity of the processes in the host. If anomaly is detected there, system automatically generates the co-stimulation.

Author: Mandot, Ekata (200211025)
Title: Traitor tracing for XML documents; x, 78 p.; 2005.
Supervisor: Mathuria, Anish
Call No.: 005.72MAN
Acc. No.: T00032
Keywords: Document language; Text processing (Computer Science); XML; Document Markup Language.
Abstract:

Electronic documents are more easily copied and redistributed than paper documents. This is a major impediment to electronic publishing. One needs to think of various copy protection schemes for the documents. There are various schemes existing for the protection of document from unauthorized users. Copy protection is very much required, once the authorized user has an access to the document. Out of two approaches, copy prevention and copy avoidance, work is done to make it difficult for the user to illegally copy the document. This effort is to make the document at least as secure as paper document. The focus is on text documents and especially XML documents. Traitor tracing is the scheme where an authorized user is caught as a traitor. This

is the domain where out of lot many authorized users; traitor has to be traced. Putting invisible marks in the document, unique for each user, i.e. fingerprinting the document is one of the techniques used to trace the traitor. Many proposals have already been made in this direction, but each deals with images and music files. A proposal is made to protect XML documents using fingerprinting. This is the Novel idea for working directly on text documents.

Author: Panchal, Niravkumar K. (200311023)
Title: Protecting Mobile Agents Against Malicious Hosts Using Trusted Computing; ix, 50p.; 2005.
Supervisor: Mathuria, Anish
Call No.: 005.84 PAN
Acc. No.: T00047
Keywords: Computer security; Intelligent agents; Mobile agents (Computer software); Mobile agents system; Trusted computing.
Abstract:

The concept of mobile agents was invented about a decade ago. Since then, plenty of innovative applications of mobile agents have been proposed. But it remains to be the fact that these applications have not been deployed to the desired extent. Security concerns associated with mobile agent systems are primary obstacles to their widespread adoption. Protecting mobile agent against malicious host is the unsolved aspect of these security concerns. Existing solutions to this problem are either not practical or not robust. We have provided a practical and robust solution to this problem using the concepts of Trusted Computing. We have designed security architecture for mobile agent systems. Our architecture uses the capabilities of the TCG (Trusted Computing Group) TPM (Trusted Platform Module) and TCG based integrity measurement architecture to provide the solution to the above mentioned problem. Since most of the mobile agent systems are Java based, we have provided an implementation of TCG aware Java Virtual Machine, which is one component of the overall architecture.

Author: Patel, Dhawal B. (200311029)
Title: Non-Uniform Information Dissemination for Performance Discovery in Computational Grids; xi, 71 p.; 2005.
Supervisor: Chaudhary, Sanjay
Call No.: 004.36 PAT
Acc. No.: T00050
Keywords: Computational grids (Computer systems); Grid Computation; Grid Computing.
Abstract:

The required service in any resource-sharing environments like Grid, Peer-to-Peer etc., is discovery of resources. A resource discovery mechanism returns locations of resources that match the description, given a description of resource desired. Two resource-sharing environments are well defined with respect to target communities, resources, applications, scalability and fault tolerance: Grid and peer-to-peer systems. Grids are sharing environments that rely on persistent, standards-based service infrastructure that allow location independent access to resources and services, which are provided by geographically distributed machines and networks. The design of the resource discovery approach must follow the rules imposed by the characteristics of grid environment. These characteristics are 1. Independence from central global control, 2. Support for attribute-based search, 3. Scalability, 4. Support for intermittent resource participation. Depending upon the types of resources that are shared, the grids can also be of different types, e.g. computational grids for the environment in which only computational resources are shared, data grids for the one in which data are shared. The focus of thesis is on performance discovery in computational grids.

Grid schedulers, that manages the resources, requires up-to-date information about widely distributed resources in the Grid. This is a challenging problem given the scale of grid, and the continuous change in the state of resources. Several non-uniform information dissemination protocols have been proposed by researchers to efficiently propagate information to distributed repositories, without requiring flooding or centralized approaches. Recently, a new concept called the "Grid potential" proposed in, as the first step towards the design of non-uniform information dissemination protocols.

In this thesis, four non-uniform dissemination protocols are analyzed for computational grids

based on the concept of "Grid potential", which follows above-mentioned requirements for resource discovery. These protocols disseminate resource information with a resolution inversely proportional to the distance of resources from the application launch point. The performance evaluation is done with respect to the dissemination efficiency and message complexity. The results indicate that these protocols improve the performance of information dissemination compared to uniform dissemination to all repositories.

Author: Ray, Anuradha (200311018)
Title: A Novel Architecture For a CMOS Low Noise Amplifier at 2.4 GHz; ix, 50 p.; 2005.
Supervisor: Parikh, Chetan D.
Call No.: 621.39732 RAY
Acc. No.: T00044
Keywords: Amplifiers (Electronics); Complementary Metal Oxide Semiconductor; Image processing; Optical data processing.
Abstract:

Radio frequency design has been one of the major research areas in the recent past. Emergence of several Wireless Communication standards has demanded availability of different analog blocks for use in transceivers with different constraints, imposed by the nature of application. Particularly, lot of research has been carried out in CMOS technology, due to its low cost nature.

LNA is one of the most important building blocks in the front end of the wireless communication systems. It determines the noise performance of the overall system, as it is the first block after the antenna. With technology scaling, the transistor's cut off frequency continues to increase, which is desirable for improving the noise performance of CMOS circuit. Some other advantages like low cost, high level of integration motivates research of RF modules using CMOS technology. In recent years valuable research is done on CMOS LNA design in submicron technologies: from topology investigation to various new ideas on improvement of low power consumption, low noise figure, high gain, smaller space and low supply voltage.

In this thesis, a new LNA architecture is reported, that consumes less power compared to other existing architectures, while providing the same gain, noise figure, CP-1dB and IIP3 figures. The new architecture achieves this better performance by combining the beneficial properties of two existing architectures – Lee's inductive input stage, and the current-reuse (or the CMOS inverter amplifier) architecture. Detailed design procedures, and Spice simulation results are presented in the thesis, along with a brief survey of noise sources in MOSFETs, and a literature survey of existing LNA architectures.

Author: Reddy, M. Vivekananda (200311015)
Title: Scheduling in Grid: Rescheduling MPI applications using a fault-tolerant MPI implementation; vi, 45 p.; 2005.
Supervisor: Chaudhary, Sanjay
Call No.: 004.36 RED
Acc. No.: T00041
Keywords: Computational grid; Grid computing; MPI-Parallel and distributed programming.
Abstract:

Due to advancement in grid technologies, resources spread across the globe can be accessed using standard general purpose protocols. Simulations and scientific experiments were earlier restricted due to limited availability of the resources. These are now carried out vigorously in the Grid. Grid environments are dynamic in nature. The resources in a grid are heterogeneous in nature and are not under a central control. So scheduling in grid is complex.

The initial schedule obtained for an application may not be good as it involves the selection of resources at a future time. The resource characteristics like CPU availability, memory availability, network bandwidth etc keep changing. Rescheduling becomes necessary under these conditions. There are many rescheduling methods in the literature. Process migration is one of them.

The thesis uses the fault-tolerant functionalities of MPICH-V2 to migrate MPI processes. Load balancing modules which make a decision of when and where to migrate a process are added into the MPICH-V2 system. Simulations are done to show that process migration is viable rescheduling technique for computationally intensive applications. The thesis also gives brief descriptions of some existing fault-tolerant MPI implementations.

Author: Reddy, S. Gangadhar (200311031)
Title: Enhancing Data efficiency in OFDM (IEEE 802.11a) using Equalization; xii, 50 p.; 2005.
Supervisor: Chakka, Vijaykumar
Call No.: 621.3821 RED
Acc. No.: T00051
Keywords: Communication network; Multiplexing; OFDM (Orthogonal Frequency Division Multiplexing); Wavelength division multiplexing.
Abstract:

IEEE 802.11a OFDM signal passed through a dispersive channel introduces ISI & ICI. To avoid ISI & ICI, cyclic prefix (guard interval) is introduced between the OFDM symbols. But the cyclic prefix contributes about 20% (0.8us/4us) of the total symbol duration. Transmission of OFDM symbols without cyclic prefix increases the data efficiency, but introduces ICI & ISI. The ISI & ICI can be removed by equalization at the receiver.

Spill over in the frequency domain is same as ICI & ISI. This spill over can be observed at the unused carriers also (carriers numbered from 0-6, 33, 59-64 are unused in IEEE 802.11a). Equalization is done in the frequency domain by making use of spill over in unused carriers. A relationship is brought between the length of the channel impulse response and the number of unused carriers for perfect equalization in the absence or very little AWGN-channel noise. To avoid the noise amplification caused by Zero Forcing equalization and to satisfy the relationship derived, a methodology using Time domain equalizer (TEQ) is proposed and simulation results are presented supporting it.

Alternatively, computational efficient algorithm for indoor environment is suggested by transmitting data in unused carriers with the combination of used carriers. By this method, ICI & ISI is removed at the transmitter itself and it even doesn't amplify the noise.

Author: Saxena, Nischal (200311030)
Title: Distributed Clustering for Heterogeneous Wireless Sensor Network in Data Gathering Applications; viii, 39 p.; 2005.
Supervisor: Ranjan, Prabhat
Call No.: 681.2 SAX
Acc. No.: T00063
Keywords: Sensor networks; Wireless communication systems; Wireless sensor networks.
Abstract:

Wireless Sensor networks have revolutionized the paradigm of gathering and processing data in diverse environment such as, wildlife area, kindergarten or agriculture farm. The nodes in these networks usually have a very low and fixed amount of energy, which cannot easily be replenished, and hence there is a need for energy efficient techniques to improve the lifetime of such networks.

Data Aggregation is one prominent method that is employed to reduce the amount of energy used in data transmission among the nodes in a network. This method requires hierarchical organization of the nodes. Clustering is one phenomenon that introduces the required hierarchy in a network. It also helps in increasing the lifetime of the network and its scalability as well. On the other hand the cost paid off for clustering is unbalanced energy consumption, which arises due to variations in the roles assigned to the nodes. This imbalance can lead to early partitioning of the network. Due to different amount of residual energy nodes cannot be considered same any more and a distinction has to be made on the basis of the residual energy and the assumption that nodes are identical has to be dropped.

This work tries to address the self-organization of a wireless sensor network in presence of heterogeneity (presence of more than one type of nodes based on the energy), which may be due to initial deployment or by the network operations. The approach suggested in this work for clustering is basically meant for the data gathering applications. It is based on the local interaction of the nodes, which accounts for scalability. The nodes that are rich in residual energy are usually elected as cluster head. The load is balanced among the nodes by periodically exchanging the roles of the nodes and attaching a node to a cluster based on a cost function, which is dependent on the distance to the cluster head, degree of the cluster head and residual energy. Work also

describes the simulation done to evaluate the performance of clustering and energy efficiency of the approach.

Author: Shah, Dhaval Kiritbhai (200311040)
Title: Model for Grid Service Instance Migration; xii, 85 p.; 2005.
Supervisor: Chaudhary, Sanjay
Call No.: 004.36 SHA
Acc. No.: T00059
Keywords: Computational grids; Grid computing.
Abstract: Grid computing, emerging as a new paradigm for next-generation computing, enables the sharing, selection, and aggregation of distributed resources for solving large-scale problems in science, engineering, and commerce. The resources in the Grid are heterogeneous and geographically distributed. The resources in the Grid are dynamic in nature. Resource owners are at discretion to submit/donate the resources in to the Grid environment. A Web Services is a network-enabled entity accessed using the standard web protocols. Web Services are basically stateless in nature and there is a need to maintain state across the transactions based on Web Services. Grid Services is an extension of Web Services in a Grid environment having statefulness as a key feature. State of any Grid Services is exposed with the help of Service Data Elements. Grid Services may fail during its life cycle due to failure of a resource or a withdrawal of a resource by the resource owner. Thus, there is a need to provide a reliable solution in the form of Grid Service instance migration to protect the work of the users, which was carried out. This thesis proposes a model that supports Grid Services instance migration. Migration of an instance can take place based on the failure of resource, increase in load at the resource, change in the policy of the domain in which resource resides, user specified migration, or migration due to withdrawal of a resource by the resource owner. It enables the users to specify the migration if (s) he does not trust the domain in which instance is running. The model includes an incremental checkpointing mechanism to facilitate migration. Thesis shows the study of checkpointing mechanism in various resource managers: condor, condor-G and LSF. It narrates the different economic models prevalent in distributed computing field. The need for dynamic scheduler for Grid is also discussed. A model for instance migration for a task having parallel independent subtask is also proposed. A proposal to modify existing Globus-GRAM protocol to support Grid Service instance migration is also suggested.

Author: Shah, Pratik P. (200311039)
Title: Active Contours in Action; viii, 48 p. 2005.
Supervisor: Banerjee, Asim
Call No.: 006.42 SHA
Acc. No.: T00058
Keywords: Active contours; Image processing; Image reconstruction; Image segmentation; Imaging systems; Optical data processing; Optical pattern recognition.
Abstract:

There was considerable success in converting images into something like line drawings without resorting to any but the most general prior knowledge about smoothness and continuity. That led to the problem of "grouping" together the lines belonging to each object which is difficult in principle and very demanding of computing. Two terms that describes this problem in image processing tasks are edge detection and segmentation.

Active contour models are proven to be very effective tools for image segmentation. The popularity of this semiautomatic approach may be attributed to its ability to aid segmentation process with apriori knowledge and user interaction. For more detailed application domain study for active contours, problem of converting a frontal photograph into a line drawing is taken up along with lip tracking based on Gradient Vector Flow force field (GVF) active contours.

In images with gaussian and salt-pepper noise, segmentation process becomes difficult for gradient based methods. This work gives a solution to this problem. A novel break n' join technique is presented and simulated for various images ranging from synthetic to real with convex and concave regions. And as an outcome, encouraging results are observed.

Author: Singh, Vivek Kumar (200311032)

Title: Knowledge Management Techniques Towards Answering Engine; vii, 74 p.; 2005.
Supervisor: Maitra, Anutosh
Call No.: 004.678 SIN
Acc. No.: T00052
Keywords: Answering search engine; Knowledge management technique; Search engine; World Wide Web.
Abstract:

The growth of Internet era has brought magnitude of information at the disposal of end user being mobilized with the speed of electron. But this bless of information comes with a curse of 'information overload'. Answer engine has come out as a well-accepted solution to this problem as it target to directly provide answer to the user's question. At present, several hurdles exist in the path of a robust answer engine capable of handling various types of complex questions and they have been mostly known as inefficient in handling natural language text. This thesis presents a study, implementation and some contribution to various aspects of this question answering approach. Notably a novel approach of summarization has been tried that works on the principle of capturing relation between salient concepts present in text. The work also presents a Feature Drift model for tracking concept drift, which is a key ingredient in construction of user model required for personalization at various stages. Finally, a representative implementation of a factoid Answer Engine and a Search Engine built for the domain of DA-IICT has been described.

Author: Sudhi, K. Venkata (200311011)
Title: Localization of Target in Wireless Sensor Networks; xi, 46 p.; 2005.
Supervisor: Chakka, Vijaykumar
Call No.: 681.2 SUD
Acc. No.: T00038
Keywords: Sensor networks; Wireless communication systems; Wireless sensor networks.
Abstract:

Advances in hardware and wireless network technology have made it possible to build and deploy dense ad-hoc wireless sensor networks of nodes collecting and disseminating information. One problem that arises in ad-hoc wireless sensor networks is the inability of the nodes to locate themselves and the object (events) as well. With a motivation to solve this, we have proposed the following in this thesis:

1. Distributed algorithm for the location of sensors having omni directional radiation pattern using MMSE distance criteria.

2. A low computational complexity grid based technique to find sub set of sensors close to the event of occurrence from the reported set of sensors to query for further information.

A MATLAB simulation is done for finding the closest sensor to the event of occurrence, without the knowledge of true positions of all the sensors in the field excluding those that act as anchors. The simulation shows a successful detection percentage of 55 with one-sensor query and 80 with two-sensor query. This detection percentage is close to the detection that is done with the knowledge of true sensor positions in the field.

Author: Suryanarayana, P. V. (200311022)
Title: Automatic Car License Plate Recognition; ix, 44 p.; 2005.
Supervisor: Mitra, Suman K.
Call No.: 621.3678 SUR
Acc. No.: T00046
Keywords: Digital image processing; Image processing; Image processing--digital techniques; Imaging systems.
Abstract:

In most traffic applications, someone gathers information manually at the scene or watching the video of a scene. With automatic car license plate recognition using image processing techniques, new ways of capturing traffic data are evolved. It works by processing a sequence of images captured by a video camera and identifying the vehicle's license plate. Locating the car license plate in an image or video frame of a car is an important step in car license plate recognition/identification applications.

In this thesis, we propose a morphology based method for license plate extraction from car images. The algorithm uses morphological operations on the preprocessed, edge images of the

vehicles. Characteristic features such as license plate width and height, character height and spacing are considered for defining structural elements for morphological operations. The localised license plates are segmented into individual character images by connected component labeling algorithm and the segmented characters of license plate are recognized by template matching approach. Entire system is implemented in Matlab and is tested over a large database of car images of various countries.

Author: Tatu, Aditya (200311027)
Title: Differential Geometry and Image Processing; viii, 49 p.; 2005.
Supervisor: Banerjee, Asim and Mitra, Suman K.
Call No.: 621.367 TAT
Acc. No.: T00049
Keywords: Differential geometry; Image processing; Image processing--digital techniques; Optical data processing.
Abstract:

There are various ways of observing and interpreting images. At higher levels of abstraction, one looks at an image as collections of objects, while at the other end it is just a collection of curves and surfaces. We study this viewpoint, through tools of differential geometry. Differential Geometry is the study of geometry using calculus. We mainly concentrate on one of its applications, active contours. Active contours are primarily used for object segmentation and object boundary detection. Traditional edge detection algorithms fail to give closed contours as object boundary when the gradient along the object edge is varying, because one may not be able to set the proper threshold for the magnitude of gradient. But active contours always give closed boundary of objects. They are of three types, parametric active contours, level set active contours and geodesic active contours. We describe the Level set active contours in detail and give a brief account of the other two.

Level set Active contours fail to detect the inner as well as outer boundary of objects with holes, using a single initial contour. This problem is stated in Weeratunga and Kamath. We have tried to solve this problem and are successful to some extent in doing so. By suitably modifying the level set contour evolution equation we have not only succeeded in detecting both boundaries of objects with holes, but also detected boundaries in case of objects with multiple holes and objects lying inside holes of other objects.

Author: Thomas, Shabu (200311013)
Title: Optimum Network Utilization using Fortz-Thorup Method; ix, 61 p.; 2005.
Supervisor: Jotwani, N. D.
Call No.: 621.3821 THO
Acc. No.: T00040
Keywords: Fortz-Thorup Method; Communication networks—Traffic; Communication networks; Data transmission modes; Network utilization; Network service provider.
Abstract:

Internet traffic has increased over the previous years and there has been a change in traffic requirements due to the emergence of new applications and services. This makes it more challenging for the network service providers to handle congestion and provide Quality of Service guarantees. Therefore, a good management and control over the functioning of a network becomes necessary. A network service provider's objective is then to have appropriate policies and mechanisms in place that ensures optimum functioning and utilization of the network such that the guaranteed service agreement with the users of the network is not violated.

This thesis work specifically focuses on increasing the utilization of a network by making use of existing capacity to carry more traffic. In this regard we propose a simple admission control scheme within the model of Fortz Thorup Method (FT Method), which avoids congestion while accommodating a new demand request. This admission control scheme tries to admit the new demand without requiring any reconfiguration of the OSPF weights thus speeding up the decision time to admit a new demand. It was found that when the network was operating in a state close to congestion as defined by the FT Method, many links were still operating below their existing capacities. New demands were created between pair of nodes, which were 1-hop, 2-hop, 3-hop and 4-hop apart and tests were conducted to check whether their admission caused congestion or

not. We found out that as the hop distance between the node-pair increased, less and less number of admission request satisfied the admission control criteria. It was also observed that, in almost all test cases, admission requests were rejected not because their acceptance caused the congestion criteria to be violated but that there was already a link in the path followed by the new request which was violating the criteria.

Author: Vege, Hari Kiran (200311003)
Title: Energy Conserving Voidless Coverage in Wireless AD-HOC Sensor Networks; vi, 44 p.; 2005.
Supervisor: Ranjan, Prabhat
Call No.: 681.2 VEG
Acc. No.: T00061
Keywords: Ad-hoc sensor networks; Wireless communication systems; Energy conservation.
Abstract:

For many sensor network applications such as intrusion detection and military surveillance, it is necessary to provide full sensing coverage to a security-sensitive area while at the same time minimizing energy consumption and extending system lifetime by leveraging the redundant deployment of sensor nodes. It is also preferable for the sensor network to provide surveillance service for target areas with different degrees of security requirements.

In this thesis, an established scheme that aims at adaptable energy-effect sensing coverage is analyzed. In this scheme, each node is able to decide a schedule for itself to guarantee a certain degree of coverage (DOC) with average energy consumption inversely proportional to the node density.

An enhancement to this scheme is suggested. The validity of the proposed extension is proved though the simulations that address the issues of total energy consumption, balance of energy consumption, half-life of the network, coverage percentage over time, energy consumption for α coverage and actual degree of coverage. Comparisons are made with the two existing schemes namely 'Adaptable Sensing Coverage Scheme' and Sponsored Coverage Scheme'.

These simulations show that the proposed scheme accomplishes α-coverage surveillance with low energy consumption. It outperforms other state-of –art schemes by as much as 50% reduction in energy consumption and as 130% increase in the half-life of the network.

Author: Asthana, Abhinav (200411033)
Title: Design and Synthesis of Asynchronous Circuits; viii, 73 p., 2006.
Supervisor: Kapoor, Hemangee K.
Call No.: 621.3815 AST
Acc. No.: T00094
Keywords: Asynchronous circuits; Asynchronous circuits--design and construction.
Abstract:

For a very long time, there has been a requirement of circuits that can overcome the difficulties caused by the delay assumptions involved in a physical system. With decreasing on-chip dimensions of circuits as a result of advancing VLSI technology, delays within the circuit interconnects have become significant. Because of these difficulties, chip manufacturing industry is in search for an alternate design methodologies such as nanotechnology and clock-less (asynchronous) circuits. Asynchronous circuits are low in power consumption, faster in speed, adaptable to newer technologies and have no global timing issues. The bottleneck with the design methodology for such circuits is the lack of automated tools and the complexity of designs. This work attempts to give an alternate synthesis °ow to the implementation of a class of asynchronous circuits, known as delay-insensitive (DI) circuits.

A recent design methodology that claims to synthesize DI circuits is \Null Conventional Logic" (NCL). Using the logical description of the design, one can implement a DI version of the circuit using NCL. As such there is no specialized language for design, verification and synthesis of NCL circuits. This work represents an effort to fill the gap by providing some translation rules for synthesis of such circuits using a language called DISP (Delay Insensitive Sequential Processes) and the NCL design methodology.

This work also incorporates the design of a programmable asynchronous shift register. This was done as a part of curiosity and exploration for understanding of the design °ow that the designers usually adopt for analyzing their designs.

Author: Ballaney, Abhishek V. (200411036)
Title: Music Genre Classification using Principal Component Analysis and Auto Associative Neural Network; viii, 39 p.; 2006
Supervisor: Mitra, Suman K.
Call No.: 006.32 BAL
Acc. No.: T00097
Keywords: Auto associative neural network; Music genre classification; Neural networks; Neural networks (Computer science)
Abstract:

The aim of music genre classification is to classify music pieces according to their style. Principal Component Analysis (PCA) is applied on raw music signals to capture the major components for each genre. As a large number of principal components are obtained for different cases, the purpose of applying PCA is not satisfied. This led to feature vector extraction from the music signal and building a model to capture the feature vector distribution of a music genre. Timbre modelling is done using Mel Frequency Cepstral Coefficients (MFCCs). The modelling of decision logic is based on Auto Associative Neural Network (AANN) models, which are feed-forward neural networks that perform identity mapping on the input space. The property of a five layer AANN model to capture the feature vector distribution is used to build a music genre classification system. This system is developed using a music database of 1000 songs spanning equally over 10 genres.

Author: Banda, Kishore Kumar (200411040)
Title: Efficient Algorithms For Hierarchical Online Rule Mining; viii, 60 p.; 2006.
Supervisor: Jotwani, Naresh
Call No.: 006.312 BAN

Acc. No.: T00101
Keywords: Algorithms; Data mining; Data mining and algorithms.
Abstract:

Association rule Mining, as one of the technologies equipped with Data Mining, deals with the challenge of mining the informative associations from the fast accumulating data. From the past decade, the research community has been busy progressing day by day towards the task of rule mining. Hierarchical Online rule mining opens a new trend to achieve an online approach in real sense. In this thesis, we further develop the theory of Hierarchical Association Rules. Notably, we propose a new algorithm that further improves the efficiency of the previously proposed works in three aspects. In phase 1 of the rule-mining problem, we introduce Hierarchy Aware Counting and Transaction Reduction concepts that reduce the computational complexity by a considerable factor. We also propose Redundancy Check while generating rules in phase 2 of the problem. We propose a modified version of a Synthetic Data Generator that deals with Hierarchical data and evaluate the performance of the proposed new algorithm. We finally discuss the issues that can form the future perspectives of the proposed new approach.

Author: Bensal, Jitendra Babu (200411012)
Title: A Low Power High Speed Amplifier Design; x, 52 p.; 2006.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.395 BEN
Acc. No.: T00075
Keywords: Amplifier (Electronics); Analog-to-digital converters; Operational amplifiers; Operational analysis; Operations research
Abstract:

The operational amplifier (op-amp) is one of the important component in analog to digital converters. The power consumption of these converters mostly depend on the op-amps used. The accuracy and speed performance of analog to digital converters can also be affected due to the finite DC gain and finite bandwidth of the opamp. So the design of op-amp is very critical for these applications.

This thesis describes the design of a telescopic operational amplifier. Of the several architectures, a telescopic operational amplifier provides better frequency response and also consumes least power in comparison with other topologies. The limited swing of the telescopic amplifier has been improved by using the current source load transistors in the linear region. Two gain boosting amplifiers are also used to enhance the gain of the amplifier. This gain boosting amplifiers uses a folded - cascode topology. The overall circuit is designed in 0.18 micron CMOS technology at a supply voltage of 1.8 Volt.

The operational amplifier achieves a dc gain of 72 dB, bandwidth of 390 MHZ, slew rate of 132 V/ µs and a differential output swing of ± 0.82 V. The overall circuit consumes a total power of 3.36 mw.

Author: Bhalerao, Mangesh (200411039)
Title: Built-In Self-Test for a Flash Analog to Digital Converter; xiii, 62 p.; 2006.
Supervisor: Parikh, Chetan D.
Call No.: 621.39814 BHA
Acc. No.: T00100
Keywords: Analog to digital converters; Metal oxide semiconductor, Complementary; System on Chips (SoCs); VLSI (Very Large Scale Integrated).
Abstract:

The intricacies of modern System on Chips (SoCs), comprising of analog, digital and even Redio-Frequency (RF) blocks on a single chip, are surpassing all previous conceivable limits. A more perplexing problem now is not the design but the testing of these SoCs, as the test costs are exceeding all other costs in manufacturing. Digital testing has burgeoned in last forty years into an almost complete science, but analog and mixed-signal and RF testing are still in a precocious state. The dearth of widely accepted standard models, methodologies and Electronic Design Automation (EDA) tools is worsening this situation.

This research work tries to suggest and implement an amelioration in Oscillation based Built-In Self-Test, for an analog and mixed signal block i.e., a high speed Analog to Digital Converter

(ADC), in deep sub-micron CMOS technology. ADCs are virtually in all modern SoCs and hence are one of the most important modules in analog and mixed-signal designs. A novel Oscillation based Built-In Self-Test is used for testing of a 3-bit 1 GHz CMOS Flash ADC, designed in 0.18 _m CMOS technology. The simulation results prove that this technique shows an excellent coverage of catastrophic as well as a good coverage of parametric faults, with minimal area overhead and lesser test time. The analog and the digital sub-systems of an ADC do not need di_erent test structure, which is its biggest advantage.

Author: Dalwadi, Gaurav Chandrakant (200411038)
Title: A 0.18µ Low Power Dual-Mode Transceiver Front-end Design for High Speed Bluetooth Systems; xii, 71 p.; 2006.
Superviso: Gupta, Sanjeev
Call No.: 621.38215 DAL
Acc. No.: T00099
Keywords: Bluetooth technology; Radio transmission receiver; Telecommunication--Equipment and supplies; Transceiver design; Wireless communication systems.
Abstract:

Today's market trend is to possess a single multi-purpose, multi-functional personal device for various wireless personal area network (WPAN) applications. So it raises a great demand to develop multi-mode/multi-standard transceiver compatible to all these applications, which is a challengeable task. Moreover, today's multi-media technology requires enhancement in speed performance. With respect to Bluetooth Standard, even version 1.2 with 1 Mbps data rate or version 2.0 + EDR with 2 or 3 Mbps data rate are not adequate considering current requirements. Bluetooth SIG has also specified another correlated standard called physical draft specifications with 4, 8 or 12 Mbps data rate to solve this issue. Currently, there are no transceivers available in the market that provides compatibility among all these versions. The core work of the thesis involves designing and analysis the multi-standard transceiver front-end system that gives compatibility with all three versions, solving RF design issues such like image rejection, flicker noise, DC offset etc. by using dual-conversion technique with choosing proper local oscillator frequency architecture. Furthermore, as Bluetooth is widely used in portable communication devices, its transceiver design requires miniaturization, long life of battery and cost-effectiveness. This thesis reports the transceiver analog front-end part designed with 0.18µ CMOS technology and 1.8 V supply. The improvement in power consumption has been obtained by implementing some recently developed low power designs of low noise amplifier, power amplifier, variable gain amplifier and limiter matching with the specifications derived through system design. Overall system and circuit-designs give very low system noise figure and hence, receiver sensitivity up to -92 dBm has been successfully achieved.

Author: Dave, Kinjal (200411034)
Title: Reconfigurable Application Specific Instruction Set Processor for Kalman Filter (R-ASIK); x, 81 p.; 2006
Superviso: Bhatt, Amit and Chakka, Vijaykumar
Call No.: 621.3815324 DAV
Acc. No.: T00095
Keywords: Electric filters, Digital; Filters; Filters, digital electronic; Kalman filtering
Abstract:

Kalman filter is one of the most important signal processing algorithms used in many tracking applications. The main challenges for hardware implementation of Kalman filter include compute intensiveness O (n3) of the algorithm, numerical sensitivity to rounding errors and huge data I/O requirements. These challenges severely limit its use in high speed, real-time tracking applications that require very small iteration times. This work proposes a novel reconfigurable architecture for the VLSI implementation of Kalman filter, coined as Reconfigurable Application Specific Instruction Set Processor (ASIP) for Kalman Filter (R-ASIK). The R-ASIK architecture is based on the concept of 'Reconfigurable Systolic Arrays (RSA)' and provides a real-time implementation by computing a single iteration of the filter in just 15(n + 1) clock cycles using only n(n+1) processing elements, where n is the order of the filter. Other unique features of R-ASIK include increased robustness to rounding errors and resolving the data I/O problem. Reconfigurable feature in R-ASIK architecture provides the flexibility of mapping filters of different sizes 'n', on the same architecture. This is a unique feature and does not exist in current literature. A novel architecture to compute transpose

of a matrix in only one clock cycle is also presented. The VLSI implementation of R-ASIK was done in three steps namely, modelling the R-ASIK using Verilog HDL, logic synthesis and physical synthesis. The implementation methodology presented for logic and physical synthesis resulted in efficient implementation of R-ASIK in silicon. R-ASIK was mapped to four target technologies (180,130, 90 and 65 nm) and the synthesis results are analyzed. Physical synthesis of R-ASIK was carried out for 180 nm technology. R-ASIK works at 50 MHz clock, which is quite high for a data path intensive algorithm like Kalman filter.

Author: Dave, Marshnil (200411020)
Title: Comparison of Single-bit and Multi-bit Second Order Sigma-Delta Modulators; x, 62 p.; 2006.
Supervisor: Parikh, Chetan D.
Call No.: 621.381536 DAV
Acc. No.: T00082
Keywords: Digital to Analog converter (DAC); Modulators (Electronics); Modulators and demodulators; Sigma-Delta Modulators.
Abstract:

This work deals with comparison of Single-bit and Multi-bit Second Order Sigma-Delta Modulators at system level for various performance metrics and different circuit nonidealities. For this work of comparison, Boser-Wooley second order sigma-delta modulator architecture was chosen for its stability and ease of implementation. Boser-Wooley singlebit and three-bit second order sigma-delta modulators employing non-ideal operational amplifiers that is operational amplifiers with finite dc gain, limited bandwidth and limited slew rate are modelled in MATLAB 6.5. The effects of these implementation imperfections on Total Harmonic Distortion, Signal To Noise Ratio and Dynamic Range of single-bit and multi-bit sigma-delta modulators are analyzed and from that the specifications of operational amplifier are derived.

The single-bit and three-bit sigma-delta modulators designed for speech applications are implemented in 0.35 micron SCMOS technology using fully differential switched capacitor circuits with dual polarity supply voltage levels. The basic analog building blocks of sigma-delta modulators like operational amplifier with Common Mode Feedback Circuit (CMFB) and comparator-latch are designed for the derived specifications, considering the design trade-offs. The switched capacitor integrators with the input stage incorporating feedback Digital to Analog Converter (DAC) is designed and implemented for three-bit sigma-delta modulator. Finally, the performance of single-bit and multi-bit sigma-delta modulators in terms of Total Harmonic Distortion, Signal to Noise Ratio and Dynamic Range is analyzed.

The behavioural modelling of sigma-delta modulators indicates that the pole error in the integrator transfer function caused by finite small signal gain of an operational amplifier increases the quantization noise floor in single-bit and three-bit sigma-delta modulators by the same amount. Small gain-errors caused by finite bandwidth of operational amplifier do not degrade the performance of single-bit as well as three-bit sigma-delta modulators. The slew rate requirement of a single-bit sigma-delta modulator is much stringent than that of a three-bit sigma-delta modulator.

Author: Dey, Nayan Kumar (200411003)
Title: A Hybrid Approach To Digital Image Watermarking Using Informed Coding, Informed Embedding and Spread Spectrum; ix, 57 p.; 2006.
Supervisor: Mitra, Suman K. and Jadhav, Ashish
Call No.: 005.8 DEY
Acc. No.: T00067
Keywords: Computer security; Digital image watermarking and spread spectrum; Digital watermarking; Watermarking techniques
Abstract:

The growth and popularity of the Internet has led to the data storage of multimedia data (audio, image and video) in digital form. The digitization form of multimedia data can be copied easily and then distributed again without the loss of fidelity. This leads to wide interest in multimedia security and multimedia copyright protection. Digital watermarking appears today as an efficient mean of securing and protecting multimedia data. It embeds a data called watermark into multimedia data such that watermark can be detected or extracted later to make an assertion about the

multimedia data. In this report, we proposed a noble hybrid watermarking scheme joining informed coding and informed embedding approach to with the most utilized spread spectrum techniques. In informed coding, the codeword used to represent a message is dependent on the cover work in which message is embedded. In informed embedding, the embedding process tailors each watermark patterns according to cover work. Our informed coding is based on trellis, which is modified so that each message can be represented by set of alternative vectors. Our scheme first embeds a watermark using informed coding and informed embedding and to increase the robustness, another spread spectrum based watermark is embedded. The watermark added to our algorithm is perceptually invisible in nature. The effectiveness of this scheme is verified through series of experiments, in which a number of standard image processing attacks are conducted. The obtained results demonstrate, proposed algorithm survives a wide range of attacks.

Author: Jain, Monika Ganpatlal (200411022)
Title: Performance Evaluation of Differentiated Services over MPLS; x, 49 p.; 2006.
Superviso: Jotwani, Naresh
Call No.: 004.66 JAI
Acc. No.: T00083
Keywords: Data switching; MPLS standard; Multi protocol; Multi Protocol Label Switching.
Abstract: There is a compelling need to provide Quality of Service (QoS) within Internet with the introduction of multimedia applications, video conferencing etc. These applications demand high resource guarantees and timeliness of data. All the existing QoS architectures such as Differentiated Services, Integrated Services, Multi protocol label switching, Constraint based routing are designed to improve the overall performance of IP networks. But since Internet is a heterogeneous network the co-existence of these architectures provides means for the delivery of end-end QoS.
Differentiated services model provides QoS by dividing the trac into various service classes and providing service differentiation to each class of trac. MPLS is a label switching technology, that does not requires longest prefix matching, thereby providing fast forwarding of packets. This research work shows that MPLS and Diffserv integration is a good model to provide QoS in backbone networks. This integrated model is capable of providing service differentiation as well as fast forwarding. As a result of which delay, which is very crucial for real time applications, is reduced. In this work various QoS elements like token bucket, leaky bucket, WFQ scheduler etc. are implemented and tested. Diffserv domain is simulated and then MPLS is build on top of it. EXP inferred LSP, where all the classes are mapped onto the same label switched path, was used for mapping of Diffserv classes onto MPLS classes. The simulation results show that performance enhancement is achieved in terms of delay reduction as well as service differentiation when we integrate the two models.

Author: Jain, Vishal (200411029)
Title: Modeling Ad hoc Network as Queuing Network; x, 50 p.; 2006.
Superviso: Srivastava, Sanjay and Lenin, R. B.
Call No.: 004.65 JAI
Acc. No.: T00090
Keywords: Ad-hoc networks; Computer networks.
Abstract: Ad hoc networks are networks in which there is no fixed infrastructure. The mobile nodes are independent and have distributed control. Modeling of Ad hoc network is a critical task, because it includes modeling of mobile behavior of nodes as well as behavior of wireless links. In this work, we propose a novel approach of modeling ad hoc network using mesh connected queuing network. We have shown that a node in Ad hoc network can be modeled as a queue receiving data from DBMAP (Discrete Batch Markovian Arrival Process) sources, which have underlying Markov chain. The packet loss probability of this queue has been simulated and found to match analytical results. The current state of art in modeling mobility in an Ad hoc network consists of selecting a velocity and direction for a node and deriving an analytical model based on these parameters. This approach lacks the concept of path and link availability. In our novel approach, data taken from various mobility scenarios through simulations are used to find out a statistical distribution that gives connectivity between two nodes. The available and unavailable duration distributions obtained from AdHocSim are incorporated into queuing network. The effect of Velocity, Area and Pause time on link availability are studied and presented. Packet error rate and Delay are

measured and validated. We show that the proposed model is useful for performance evaluation and parameter tuning of existing routing protocols.

Author: Katare, Aradhana (200411024)
Title: Content-Based Image Retrieval System for Multi-Object Images Using a Combination of Features; viii, 49 p.; 2006.
Supervisor: Mitra, Suman K. and Banerjee, Asim
Call No.: 006.7 KAT
Acc. No.: T00085
Keywords: Content based image retrieval (CBIR); Image processing--digital techniques; Multi object image database; Multimedia systems.
Abstract:

Content-based image retrieval (CBIR) is a research area dedicated to address the retrieval of images based on automatically derived features from the content of the images in database. Traditional CBIR systems generally compute global features of the image for example, based on color histograms. When a query images is fired, it returns all those images whose features match closely with the query image. The major disadvantage of such systems based on global features is that they return the images that match globally but cannot possibly return images corresponding to some particular objects in the query image.

The thesis addresses this problem and proposes a CBIR system for multi object image database with 3D objects using the properties of the object in the images for retrieval. Object segmentation has been achieved using GVF Active Contour. An inherent problem with active contours is initialization of contour points. The thesis proposes an approach for automatic initialization of contour points. Experimental results show that the proposed approach works efficiently for contour initialization. In the thesis in addition to shape feature using modified chain code other features for object retrieval using colour with the aid of colour moments and texture using Gabor Wavelets have also been used. A comparative study has been made as to which combination of features performs better. Experimental results indicate that the combination of shape and color feature is a strong feature for image retrieval.

Author: Kaushik, Gaurav (200411025)
Title: Receiver Amplifier Design Using CMOS Current Feedback Amplifier & Current Conveyors; xi, 51 p.; 2006.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.39732 KAU
Acc. No.: T00086
Keywords: CMOS (Electronics); Complementary metal oxide semiconductor; Metal oxide Semiconductors, Complementary
Abstract:

In the world of high-speed communications, systems involving high-speed data transfer require circuits with innovative features for good performance in terms of speed and power consumption. These data transfer systems constitute of large number of data channels each constituting of driver unit, transmission lines and a receiver unit. The receiver unit has small differential signals as the input. The designed receiver amplifier is required to have wide bandwidth, large slew rate and at the same time, capability to convert the differential input signal to single ended amplified signal without much distortion. For large number of data channels, it is also required that the power consumption of the receiver unit is minimal.

In this work, a model for the receiver amplifier design is implemented using a closed loop amplifier and a differential to single ended converter. Current feedback amplifier is selected for the design of the closed loop amplifier due to their advantages over other topologies in high-speed design. Current feedback amplifiers have current on demand architecture that provides them dynamic current from the supply rails for charging or discharging load for large input signals. The differential to single ended converter is designed using two translinear positive second generation current conveyors. Translinear current conveyors due to their simple circuitry and dynamic current supply during large input signals are able to provide large bandwidth and low loss of signal resulting in very high-speed signal processing.

The amplifier model is implemented in MOSIS 0.5 μm single-well technology using BSIM 3.0

model parameters. The obtained results are discussed in the end along with comments on the performance of the current mode circuits involved – current feedback amplifier and current conveyor.

Author: Kulkarni, Vineet (200411015)
Title: A Two-level Pricing Scheme for Congestion Control and Service Differentiation in the Internet; ix, 62 p.; 2006.
Supervisor: Srivastava, Sanjay and Lenin, R. B.
Call No.: 004.678 KUL
Acc. No.: T00078
Keywords: Internet (World Wide Web); Internet and scheme; Internet service pricing; Internet--Computer programs; Internet service provider; Internet users; Pricing mechanism; Pricing scheme.
Abstract:

It is the property of any good service provider that, if a user is ready to pay for the services he demands, the provider will ensure that the requested level of service is made available. Is this possible in the Internet? The answer is No. This is because there is no uniform economic model based on which service is provided in the Internet. Through pricing, we provide one such model which is sensitive to user demands and budgets.

The proposed pricing mechanism performs the dual functions of providing service differentiation according to budgets, and doing congestion control through feedback at time scale comparable to a round trip time. We investigate the optimal rate allocation and stability issues of the proposed scheme.

A two level pricing scheme is proposed to reflect the structure of the Internet. Data statistics are maintained as an aggregate, thus reducing the load on intermediate routers in the Internet. The scheme has been proposed so as to require minimal changes to the current Internet. The working of the pricing scheme in different traffic scenarios is demonstrated through simulations.

Author: Malviya, Yogesh (200411014)
Title: Extremely Low Voltage Operational Amplifier Design with Rail-to-Rail Input Common Mode Range; vi, 36 p.; 2006.
Superviso: Nagchoudhuri, Dipankar
Call No.: 621.395 MAL
Acc. No.: T00077
Keywords: Amplifiers; Amplifiers--electronics circuits; Amplifier (Electronics); Amplifier design; Operational amplifiers
Abstract:

Increasing trends towards battery operated systems demand circuits to be designed at low voltages. Low voltage operation severely limits the operational amplifier as a voltage buffer as the input common mode range available is very limited. This work deals with designing a very low voltage amplifier that can be used as a unity gain buffer. The architecture is based on using an operational amplifier in conjunction with an adapter circuit. The compliance voltage of the tail current source is maintained constant by comparing with a reference voltage using negative feedback action. The amplifier has been designed in 0.18μm technology at a supply voltage of 0.8 Volts. The amplifier gives a constant performance for varying common mode voltage as is demanded for a rail-to-rail amplifier. Designed amplifier gives a gain of 77.4dB with an input stage transconductance 'Gm' variation of just 1.29 % over the entire input common mode range.

Author: Manwani, Naresh (200411002)
Title: Gaussian Mixture Models for Spoken Language Identification; viii, 57 p.; 2006.
Supervisr: Mitra, Suman K. and Joshi, Manjunath
Call No.: 621.3994 MAN
Acc. No.: T00066
Keywords: Automatic speech recognition; Gaussian mixture models; Language identification; Speech perception; Speech recognition; Speech recognition, automatic.
Abstract:

Language Identification (LID) is the problem of identifying the language of any spoken utterance irrespective of the topic, speaker or the duration of the speech. Although A very huge amount of

work has been done for automatic Language Identification, accuracy and complexity of LID systems remains major challenges. People have used different methods of feature extraction of speech and have used different baseline systems for learning purpose. To understand the role of these issues a comparative study was conducted over few algorithms. The results of this study were used to select appropriate feature extraction method and the baseline system for LID.

Based on the results of the study mentioned above we have used Gaussian Mixture Models (GMM) as our baseline system which are trained using Expectation Maximization (EM) algorithm. Mel Frequency Cepstral Coefficients (MFCC), its delta and delta-delta cepstral coefficients are used as features of speech applied to the system. English and three Indian languages (Hindi, Gujarati and Telugu) are used to test the performances. In this dissertation we have tried to improve the performance of GMM for LID. Two modified EM algorithms are used to overcome the limitations of EM algorithm. The first approach is Split and Merge EM algorithm The second variation is Model Selection Based Self-Splitting Gaussian Mixture Leaning We have also prepared the speech database for three Indian languages namely Hindi, Gujarati and Telugu and that we have used in our experiments.

Author: Mohanty, Swaprakash (200411035)
Title: Design of a low power, high speed MAC unit; xiii, 77 p.; 2006.
Superviso: Nagchoudhuri, Dipankar
Call No.: 621.3822 MOH
Acc. No.: T00096
Keywords: Digital signal processing.
Abstract:

MAC operation is the main computational kernel in any digital signal processing architectures. MAC consumes nearly 2/3 portion of total power dissipated in a DSP block. This thesis deals with the design of a low power, high-speed MAC unit using custom based approach. Power-delay product (PDP) is taken as a design metric for this thesis. To meet the objective the first step is to design low power and speed efficient sub-blocks of a MAC unit such as Full Adder, register, multiplexer etc. Five different types of MAC units are designed. They are MAC unit using modified Booth's algorithm, MAC unit using carry save principle, MAC unit using bypass principle and reconfigurable MAC unit. A performance analysis is drawn among these architectures. MAC unit is implemented using both conventional full adders as well as using a low power, high-speed full adder architecture. Layout of MAC unit architectures are done using Magic tool (0.25µm technology as well as 0.18 µm technology). Power & timing analysis are done using LTSpice & Irsim tool. After simulation it is concluded that MAC unit designed using bypass principle and reconfigurable MAC unit are suitable for low power DSP applications.

Author: Nimmagadda, Prathyusha (200411016)
Title: Automation of Model Based Estimation Filters; vii, 46 p.; 2006.
Supervisor: Chakka, Vijaykumar
Call No.: 621.3815324 NIM
Acc. No.: T00079
Keywords: Electric filters, digital; Filters; Filters, digital electric; Model based distributed systems
Abstract:

Model based estimation filters are widely used in the field of estimation. They are applied for various types of dynamic and measurement models. There are different ways of solving these model based state estimation problems.

The different methods available are analyzed, giving a detailed discussion of the different levels of automation available. A model is proposed for obtaining a higher level of automation.

In this thesis, the various problems, that are to be faced while making the model based state estimation problems automatic, are discussed. A solution is proposed for over coming these difficulties, which is supported by the results obtained.

Author: Patel, Deven (200411028)
Title: Bandwidth Compression; vii, 35 p.; 2006.

Supervisor: Sahasrabudhe, S. C.
Call No.: 621.3881 PAT
Acc. No.: T00089
Keywords: Bandwidth compression, television; Television bandwidth compression.
Abstract:

Bandwidth compression implies a reduction in bandwidth of an information carrying signal without reducing the information content of the signal. Methods such as PCM, DPCM and other redundancy removal algorithms rely on the sample-by-sample values of the signal. The work described in the thesis looks at the possibilities of encoding the sequences using shorter description, based on their second order moments. A Markov model is the simplest realization of an information source. As proved by the Asymptotic Equipartition Property [Sha48], not all sequences are produced with the same probability by such a source. Only a fraction of the total sequences is produced with a high probability. The number of these high probability sequences decide the number of bits required to represent these sequences. The number of these sequences are calculated for different models. An estimate of autocorrelation for lag 1 of these sequences is then made. The results then show that the bit rate reduction increases with the correlation coefficient.

Author: Patel, Hima M. (200411001)
Title: A Study of Face Recognition Systems; viii, 43 p.; 2006.
Supervisor: Mitra, Suman K
Call No.: 006.4 PAT
Acc. No.: T00065
Keywords: Face recognition--Human (Computer science); Pattern classification systems; Pattern recognition computers; Pattern recognition systems.
Abstract:

Face Recognition comes under the general area of object recognition and has attracted researchers in the pattern recognition community for the past thirty years. The significance of this area has grown rapidly largely for surveillance purposes. This thesis is on a study of face recognition techniques. Three new algorithms have been proposed, implemented and tested using standard databases and encouraging results have been obtained for all of them.

The first algorithm uses modular Principal Component Analysis (PCA) for feature extraction and a multi class SVM classifier for classification. The algorithm has been tested for frontal face images, face images with variations in expression, pose and illumination conditions. Experimental results denote a 100% classification accuracy on frontal faces, 95% accuracy on expression variation images, 78% for pose variation and 67% for illumination variation images.

The next algorithm concentrates solely on the illumination variation problem. Edginess method based on one dimensional processing of signals is used to extract an edginess map. Application of PCA on the edginess images gives the weight vectors which are used as features to a multi class SVM classifier. An accuracy of 100% has been obtained, proving the method to be tolerant to illumination variations.

The final part of the thesis proposes a bayesian framework for face recognition. The nodes of the bayesian classifier are modelled as a Gaussian Mixture Model (GMM) and the parameters of the nodes are learnt using Maximum Likelihood Estimation (MLE) algorithm. The inferencing is done using the junction tree inferencing algorithm. An accuracy of 93.75% has been achieved.

Author: Patel, Jay (200411030)
Title: Statistical Delay Modeling and Analysis for System on Chip; vii, 49 p.; 2006.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.395 PAT
Acc. No.: T00091
Keywords: Integrated circuits; System on Chip; VLSI (Very Large Scale Integrated).
Abstract:

It is seen that designing using conventional methodologies in Deep Sub Micron geometries, at times, ends up in very pessimistic design and less yield. This is because, today's tools don't consider statistical variation of parameters in the fabrication process. IC manufacturer can give probability distribution of such parameters. Using those distributions the tool to be designed will

give the probability distribution for delays and slacks. A probabilistic estimation can be made about design functioning in deep sub micron geometries. The delays will have probability distributions based on the parameter variations. These distributions can be found using the way of SPICE simulations. But when circuit complexity increases, these simulations will take a lot of time and it is not the suitable way for large designs. A quick and efficient model has been developed based on MOSFET characteristics. Moreover, a statistical delay model for propagation delay of a gate has also been worked out. Also new methodology and implementation scheme is proposed.

Author: Patel, Komalben (200411013)
Title: Mobility Aware MANET Routing Protocol using Cross Layer Design; vii, 52 p.; 2006.
Supervisor: Srivastava, Sanjay and Lenin, R. B.
Call No.: 004.65 PAT
Acc. No.: T00076
Keywords: Ad-hoc wireless networks; Computer networks; Mobile Ad-hoc Networks; Routers (Computer networks); Routing protocol; Wireless communication systems.
Abstract:

Mobile Adhoc Network (MANET) is a dynamic network with time varying topology and time varying network resources. Due to the error-prone wireless channel and high mobility, traditional protocols of wired networks cannot be successfully applied to MANETs. The popularity of mobile and hand held devices equipped with wireless interface is creating a new challenge for Quality of Service. The wired network has also not been able to fulfill end-to-end guarantees. Due to the nature of MANETs, achieving the same end-to-end guarantees is very difficult. The mobility rate makes the task dicult. The aim is to fight against the losses caused due to mobility. This work attempts to build stable paths so as to counter the effects of mobility induced route failures. Using the Cross Layer Approach, the signal strength of the link from the MAC Layer is captured and used at the network layer. Upon receiving the signal strength values, the network layer carries out a prediction mechanism to predict the future signal strength. This information is then used to categorize the link as stable or unstable. The work also deals with designing a proactive routing protocol which uses the information of stable and unstable links to build up routes using limited dissemination technique. The protocol is similar to distance vector protocol in which, only the distance vectors whose next hop is a stable is advertised. This ensures that only stable link information reaches the other nodes in the network. The protocol has been tested in Network Simulator-2 and compared with the Destination Sequenced Distance Vector [PB94] and the Adhoc On-Demand Distance Vector [PR97] protocols. Various parameters like percentage of packet delivery, packet latency, effects of moblity, etc. are measured. The results show that the performance of the designed protocol is better than AODV in high traffic scenarios. With less overhead, the proposed protocol always performs better than DSDV. In high mobility scenarios, the protocol is comparable to AODV and performs better than DSDV.

Author: Purohit, Amit Gopal M. (200411032)
Title: A Linearity Enhancement Technique for Low Noise Amplifiers; xii, 52 p.; 2006.
Supervisor: Gupta, Sanjeev
Call No.: 621.38132 PUR
Acc. No.: T00093
Keywords: Amplifiers (Electronics); CMOS Technology; Low noise amplifiers; Low noise amplifiers technique.
Abstract:

The development of CMOS technology in to deep sub micron enables the use of such technology for implementation for GHz RF circuits. Personal communication needs a low cost and low noise RF transceiver for cellular applications using CMOS technology. Low Noise amplifier is one of the basic building blocks in any receiver system. The LNA determines the overall system's noise performance, as it is first gain block after antenna. LNA must amplify the input signal with lowest noise possible because it decides the whole device's performance under noisy signal. In order to have high receiver sensitivity the LNA is required to have not only low noise figure but also high gain and low input VSWR.

Normally, LNA design involves the tradeoff between noise figure, gain, linearity and power consumption. Consequently, the goal of LNA design is to meet system requirements with minimum noise figure and highest possible linearity. This thesis attempts to propose a linearity enhancing

technique to simultaneously match high linearity and low noise figure requirements. The design is based upon the third order intermodulation product (IM3) and output current equations of MOSFET when it is subjected to an ac input signal. By using these expressions, the design principle and advantages for the mentioned LNA technique are explained.

In this thesis a linearity enhancement technique is proposed which increases third order intermodulation product of low noise amplifier (IIP3) up to +10 dBm without a large increase in overall noise figure. Input impedance of low noise amplifier is matched to 50Ω while output impedance is kept high and unmatched. Prelayout simulation results, layout and postlayout simulation results are given to show that the technique really works satisfactory and gives good linearity.

Author: Purohit, Shakti Gopal M. (200411031)
Title: Resource Discovery in Computational Grids: Quantitative Comparison and Analysis of MDS and DHT; viii, 54 p.; 2006.
Supervisor: Chaudhary, Sanjay
Call No.: 004.36 PUR
Acc. No.: T00092
Keywords: Computational grid (Computational systems); Grids, Computational (Computer system); Monitoring and discovering computer system.
Abstract:

Grid Information Services provided by most of the grid middlewares aim at discovering resources in wake of large number of Grid nodes. Many Grid Information Services (GIS) have been deployed in different Grid middlewares. While deploying a Grid, it is a challenging task for the Grid administrator to opt for the GIS which performs better. Till date not many results exist to support such decision making. This work aims to provide the behavior and performance of two most widely deployed GIS viz. Monitoring and Discovery Services (MDS) and Distributed Hash Tables (DHT). A quantitative comparative analysis of the two schemes has been performed.

Experiments have been designed and performed over GridSim, to understand the behavior of the two services in presence of large number of users and resources. Four experiments are conducted, scalability of the two schemes has been studied, and the parameters that form bottlenecks in the behavior of these two schemes have been identified. Upper bounds have been established over the parameters identified, e.g. number of users an index server can support, number of information providers, response time and throughput which affect the performance. Finally the results obtained establish that DHT index server scales better and provide higher throughput as compared to MDS index server. The results provide an aid in deploying of the information services and help in future development work.

Author: Rana, Deepika (200411021)
Title: Detection of Unauthorized Vehicle Movement across the Forest Boundary using Wireless Sensor Networks; ix, 66 p.; 2006.
Supervisor: Srivastava, Sanjay and Lenin, R. B.
Call No.: 681.2 RAN
Acc. No.: T00102
Keywords: Forest boundary; Sensor networks; Vehicle movement; Wireless sensor networks.
Abstract:

Wireless sensor network is a collection of small sensor nodes. These nodes consist of sensing, communication and computation capability that attracts a large number of applications. Wireless sensor networks are deployed for a particular application on hand and are therefore application-specific in nature. An effort has been made in this thesis work to understand the true potential of such networks by studying the on-going work in this field. A novel application has been identified that would benefit from the deployment of such network. Presence of unauthorized vehicle inside the forest premises can be detected and its information can be made available to the forest officials. Sensor network architecture has been designed for the application. Importance of placement of sensor nodes and scheduling the sensor nodes to achieve longer lifetime are also discussed. Simulation results show how the system behaves under various conditions.

Author: Rao, A. Narayana (200411004)
Title: Low power high slew-rate adaptive biasing circuit for CMOS amplifiers; ix, 47 p.; 2006.
Supervisor: Parikh, Chetan D.
Call No.: 621.39732 RAO
Acc. No.: T00068
Keywords: CMOS (Electronics); Complementary Metal Oxide Semiconductor; Metal oxide semiconductors, Complementary.
Abstract:

Adaptive biasing technique in analog and mixed signal integrated circuit design is used mainly to reduce the power and improve the driving capability. It has found many applications, like power amplifiers in RF communication systems whose biasing current is adjusted based on the detected input RF signal level. In RF tuning circuits filters can be automatically tuned simply by varying the bias current of the transconductance amplifier with respect to the control voltage. Existing techniques uses different methods like dynamically switching the current, using feed back, etc. Some of these are area efficient techniques and some are power efficient techniques. In this work, a new adaptive biasing scheme is proposed which shows excellent results in terms of both area and power without affecting amplifier design. It uses a simple input pair to sense input signals, current mirrors to generate a difference between two currents, this difference in current varies linearly with the input signal while nonlinearity is cancelled out. Simulation results shows about 80% of quiescent power can be saved while maintaining the amplifier small signal characteristics.

Author: Shah, Malav (200411005)
Title: Efficient Scan-Based BIST Scheme for Low Heat Dissipation and Reduced Test Application Time; viii, 56 p.; 2006.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.395 SHA
Acc. No.: T00069
Keywords: BIST- Built-in-self test; Integrated circuits--Very large scale integration--Testing; VLSI (Very Large Scale Integrated).
Abstract:

Switching activity during test application can be significantly higher than that during normal circuit operation in many circuits. This is due to the fact that the correlation between consecutive test vectors is significantly lower than that between consecutive vectors applied to a circuit during its normal operation. Circuits are increasingly tested at higher clock rates, if possible, at the circuit's normal clock rates (called at-speed testing). Consequently, the heat dissipation during test application is on the rise and is fast becoming a problem that requires close attention to avoid damaging CUTs. The use of scan DFT can further decrease the correlation between successive vectors applied to the next state inputs. This may lead to hazardous effects such as excessive heat dissipation, increased electro-migration rate and higher ground bounce noise that seriously affects the reliability of the circuit leading to unnecessary loss of yield.

This work presents a simple yet efficient low hardware overhead testing scheme for scan-based built-in self-test (BIST) architecture that reduces switching activity in CUTs and test application time without compromising in the fault coverage. Firstly demonstrated is the existing Low Transition Random TPG (LT-RTPG) based test-per-scan scheme targeted for low heat dissipation during test by reducing the number of transitions at the cost of reduced fault coverage. A combined approach using both test-per-scan and test-per-clock application schemes is presented. This improves the fault coverage but at the cost of losing away, to a great extent, the advantage of lesser transitions that was gained using the low transition TPG. Given later is the proposed BIST capability built on top of a partial scan circuit adding above LT-RTPG as the TPG and MISR for signature analysis. This takes optimum advantage of the combined approach. Results show that the proposed BIST scheme gives satisfactory fault coverage (almost comparable to conventional LFSR) that too, with a large reduction in test lengths and transitions.

Author: Shah, Nishit H. (200411018)
Title: Integrated Chaos Generator; viii, 54 p.; 2006.
Supervisor: Nagchoudhuri, Dipankar

Call No.: 621.3822 SHA
Acc. No.: T00081
Keywords: Analog to digital converter; Chaotic signals; Choas theory; Signal processing.
Abstract:

With the explosion of information, the need to cater to the demands of increased number of users is of paramount importance. Spread Spectrum Technique used in wideband communications have proved to utilize the limited communication resources efficiently to meet the need of the hour. This technique requires the generation of large number of secure, orthogonal codes that can be allotted to each user. Chaotic signals being deterministic, aperiodic, broadband but dicult to predict over a longer duration qualify to be ideal candidates to generate the required pseudo random codes.

This work is focussed at generating chaotic signals in continuous time as well as in discrete time simultaneously. These signals are generated by iterating through the Modified Bernoulli Map due to its simplicity, ease of physical realization and reliability. This has been implemented through switched capacitor circuits performing the sample and hold function and residue amplification. A two stage fully differential telescopic cascode Op-Amp has been designed to meet the specifications of gain, unity-gain bandwidth and slew rate as an integral part of switched capacitor circuits. The topology also incorporates a coarse analog to digital converter(ADC) along with an encoder in feedback loop to account for the discontinuities in the map.

Verification of the generated chaos from the system has been done on the basis of its time domain evolution, correlation properties and power spectral density. This has also been compared with the ideal system implementing the same map on similar grounds. The work has been carried out in 0.35µm, bipolar supply, N-well technology using BSIM 3v3.1 SPICE model parameters for simulations.

Author: Shah, Parag (200411026)
Title: Decoupling Delay and Bandwidth in Stateless Core Networks; x, 58 p.; 2006.
Supervisor: Jotwani, Naresh
Call No.: 621.38215 SHA
Acc. No.: T00087
Keywords: Communications network architecture; Computer network architecture; Network architecture; Stateless core networks.
Abstract:

The use of network applications like VoIP, video conferencing and online stock marketing has greatly increased over the past few years. These applications require performance bounds on bandwidth, delay and delay variations otherwise they become useless. The solutions proposed by IETF, an authorized Internet body, for providing performance guarantees are not in favor of Internet's scalability and robustness. In an attempt to provide guaranteed services Dr. I. Stoica had proposed the Stateless Core (SCORE) architecture as a part of his doctoral work at CMU. The SCORE can support all functionalities of the current Internet. Moreover, it can support guaranteed services proposed by IETF without affecting current Internet's scalability and robustness. Core Jitter Virtual Clock (CJVC) is the scheduling discipline that provides absolute service guarantee in SCORE domain. The delay bound provided by CJVC depends on the reserved rate of the flow. The coupling of delay and bandwidth is considered to be a drawback of CJVC as the flows requiring low delay bound need to reserve large bandwidth. The well-known stateful guaranteed service disciplines like Weighted Fair Queueing (WFQ) and Delay Earliest Due-Date (D-EDD) also have the same problem. Several solutions like Service Curve based Earliest Deadline (SCED) and Rate Controlled Static Priority (RCSP) have been proposed for the mentioned coupling problem but they are limited to stateful networks. In this thesis, we propose a new scheduling discipline for the same problem but in stateless core network. The proposal is to emulate RCSP scheduling discipline algorithm in SCORE domain. Basic admission control algorithm has also been proposed in the course of emulating the behaviour of RCSP in SCORE architecture.

Author: Singh, Archana (200411023)
Title: Speech Driven Facial Animation System; x, 45 p.; 2006.
Supervisor: Jotwani, Naresh
Call No.: 621.3994 SIN

Acc. No.: T00084
Keywords: Co-articulation; Facial animation system; Frame; Gaussian mixture model; Hidden markov model; Speech recognition; Vector quantization; Viseme; Viterbi Algorithm.

Abstract: This thesis is concerned with the problem of synthesizing animating face driven by new audio sequence, which is not present in the previously recorded database. The main focus of the thesis is on exploring the efficient mapping of the features of speech domain to video domain. The mapping algorithms consist of two parts: building a model to fit the training data set and predicting the visual motion with the novel audio stimuli. The motivation was to construct the direct mapping mechanism from acoustic signals at low levels to visual frames. Unlike the previous efforts at higher acoustic levels (phonemes or words), the current approach skips the audio recognition phase, in which it is difficult to obtain high recognition accuracy due to speaker and language variability.

Author: Singh, Ram Sahay (200411027)
Title: Implementation of Constant gm CMOS op-amp input stage using overlapping of Transition region in 0.18µm Technology; x, 44 p.; 2006.
Supervisor: Parikh, Chetan D.
Call No.: 621.39732 SIN
Acc. No.: T00088
Keywords: Analog circuit design; CMOS (Electronics); Metal oxide semiconductors, Complementary.

Abstract: Operational amplifier is the backbone of most of analog circuit design. For low voltage applications, op-amp should have a rail-to-rail common mode input voltage. This report describes the implementation of a constant gm rail-to-rail CMOS op-amp using complementary input pairs, at 0.18µm MOS technology. The concept used to make the input transconductance (gm) constant is the overlapping of transition regions of n-pair and p-pair tail transistors using a DC level shifter [2]. A constant gm input stage insures a uniform frequency response for the entire common mode input range. It also improves the Common Mode Rejection Ratio (CMRR). The results of the designed op-amp show that it has a rail-to-rail input common mode range and a rail-to-rail output voltage swing. For rail-to-rail output voltage swing a Class AB output stage is used. Layout of the chosen architecture is made using 0.18µm technology. Comparisons of pre-layout and post-layout simulation results are done.

Author: Soni, Maulik (200411011)
Title: Distributed Caching Mechanism for Video On Demand on the Internet; ix, 55 p.; 2006.
Supervisor: Srivastava, Sanjay and Lenin, R. B.
Call No.: 004.53 SON
Acc. No.: T00074
Keywords: Chache memory; Computer storage devices; Distributed chaching mechanism; Memory (Computer science); Video on demand.

Abstract: Video on Demand applications in the Internet are delay sensitive and highly resource intensive applications. Such applications require streaming of large video files in a time bound manner. Because large volume in terms of data and high transmission rate video streaming requires high bandwidth and storage space than data transfer applications. Caching an ongoing stream at an intermediate node between the content server, which provides video on demand service, and the client(s) is a viable solution to save resources.

The proposed scheme is such a caching scheme, which caches video content among the intermediate nodes in a distributed manner. The streams are cached among the dynamically selected caching nodes and the clients are served the video content from these nodes. The caching nodes contact each other and collaboratively act together to provide the service. The scheme also proposes a heuristic to estimate resource requirements for the video on demand systems.

The behavior of the scheme is demonstrated through simulation. The quality of service using the proposed scheme is compared with some of the existing schemes.

Author: Swarnkar, Hemant (200411006)
Title: Passive Direction of Arrival (DOA) Tracking; vii, 50 p.; 2006.
Supervisor: Chakka, Vijaykumar
Call No.: 621.38412 SWA
Acc. No.: T00070
Keywords: Control theory; Estimation theory; Filtering, Kalman; Passive direction; Radio engineering; Stoachastic process.

Abstract:

The work reported in this thesis is concerned with the Passive Direction Of Arrival (DOA) tracking problem. Traditionally model based approach is used to solve tracking problems. The measurements (DOA) are nonlinearly related to position (element of state model) and does not include any range information. This makes the tracking problem very complex. Since we also have to deal with the effects of noise and sensor uncertainties, this results in a potentially unobservable nonlinear estimation problem.

Estimation of position of target from DOA measurements which has nonlinear relation with state vector, demands the use of a linearized model approach.

The whole thesis work has been divided into two part. First part analyzes the observability problems of DOA tracking i.e. it analyze the given scenario for the unique solution and suggest some correction to get proper system parameter estimation. This part also tries to find the principle causes of filter divergence.

In second part, the thesis is concentrated on the estimation methods used to track target. In this part thesis analyzes two different estimation algorithms named Extended Kalman Filter(EKF) and Pseudo Linear Estimator(PLE).

Thesis proposed a Triangulation Estimator which estimates the target motion parameter by using the geometry formed by the target and sensors available. Finally thesis compared the performances of the algorithms considered in it on the realistic underwater scenario.

Author: Tandon, Manu (200411010)
Title: FM Based Pipeline ADC; 60 p.; 2006.
Supervisor: Parikh, Chetan D.
Call No.: 621.39814 TAN
Acc. No.: T00073
Keywords: Amplifier (Electronics); Analog electronic systems; Analog to digital converters; Frequency modulation (FM) systems; Operational amplifiers; Operational analysis

Abstract:

This thesis aims at designing a new architecture for an FM based pipelined Analog to Digital Converter (ADC). It is based on the fact that power is a function of voltage and therefore handling with voltage becomes a difficult task when trying to achieve low power consumption. The idea is to change the very basis on which an ADC works, that is voltage. For frequencies can be generated up to large values without much power consumption. FM based Flash ADCs have been worked upon with power and size reduction for the last decade. An FM based pipelined ADC consists of a mixer and a frequency comparator. The comparator functions by filtering and then converting the signal to a DC value, followed by a digital inverter. The inverter decides the flipping action to zero or one. The mixer is a passive one which generates a subtracted signal with other harmonics as well. As inverter is the only active component and hence this ADC is suitable for low power applications.

Author: Trivedi, Ronak (200411037)
Title: Low Power and High Speed Sample and Hold Circuit; 49 p.; 2006.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.39814 TRI
Acc. No.: T00098
Keywords:

Abstract: In this thesis work the design of a high speed and low power CMOS sample and hold circuit as a front-end block of pipelined analog-to-digital converter is described. The circuit consists of bottom-plate sampling with differential architecture of Operational Transconductance Amplifier. The sample-and-hold circuit has been laid out in 0.18 µm CMOS technology and simulated using MOSIS CMOS BSIM3v3.1 SPICE parameters. The measurement result shows that the SFDR of 65 dB is achieved up to the sampling frequency of 100 MSPS for input signal amplitude of 1.2 Vpp. The sample-and-hold circuit consumes 4.7 mW from a 1.8 volt supply.

Author: Vadnala, Praveen Kumar (200411007)
Title: Secure and Efficient Key Assignment Scheme for Dynamic Access Control in a Hierarchy; ix, 66 p.; 2006.
Supervisor: Mathuria, Anish
Call No.: 005.8 VAD
Acc. No.: T00071
Keywords: Computer security; Cryptography; Key assignment scheme.

Abstract: The users belonging to an organization are often assigned different access permissions depending on their security class. In this situation, the users belonging to a higher security class are allowed access to the information accessible to the users belonging to a lower security class, but the opposite is not allowed. In the past two decades, many cryptographic solutions to the hierarchical access control problem have been proposed. This thesis classifies the existing schemes depending upon different properties such as type of hierarchy, key derivation method, the range of applications, etc. A comparative analysis of some prominent schemes is presented. Attacks are proposed on an existing scheme due to Yang and Li. A modification is proposed to avoid the attacks and improve the efficiency of the scheme. The modified scheme is proved to be secure using a security model proposed by Wu and Wei. A countermeasure is proposed to overcome an attack on an existing time-bound scheme due to Tzeng.

Author: Verma, Aseem (200411017)
Title: Design of a Low power high slew rate OPAMP and to study its impact on Sigma Delta Modulator's performance; xi, 66 p.; 2006.
Superviso: Parikh, Chetan D.
Call No.: 621.39732 VER
Acc. No.: T00080
Keywords: Amplifier (Electronics); CMOS (Metal oxide semiconductors, Complementary); Operation research; Operational amplifiers; Operational analysis.

Abstract: This thesis presents the work done on the design of a low-power, high slew rate opamp and subsequently the design of a fully-differential second order Switched-Capacitor architecture of a Sigma Delta modulator in 1.8 V, 0.18 micron CMOS process.

A nonsaturated differential input stage is used as an adaptive bias circuit in a Super Class AB opamp, implemented in fully-differential configuration using high swing cascade mirrors. Comparator and clock generating circuit are also designed for the modulator.

Various design aspects such as clockfeedthrough, charge injection and KT/C noise have been taken into consideration while designing the modulator.

Inaccurate and Incomplete charge transfer in integrator due to bandwidth and slew rate limitations results in gain error and harmonic distortion respectively in the modulator output. Thereby reducing the Signal to Noise and Distortion Ratio of the modulator. Hence Slew rate must be large enough so that the distortion introduced falls below the noise floor of the modulator.

Simulation results show that the amplifier has a very small static power dissipation of 0.54 mW, it can supply a maximum output current of 0.65 mA and static power dissipated by sigma delta modulator is 2.7 mW.

Author: Vij, Aditya (200411008)

Title: Low Power BIST Architecture for Fast Multiplier Embedded Core; ix, 42 p.; 2006.
Superviso: Nagchoudhuri, Dipankar
Call No.: 621.395 VIJ
Acc. No.: T00072
Keywords: BIST (Built in self test); Circuits; Circuit testing; Integrated circuits--Very large scale; Test pattern generators; VLSI (Very Large Scale Integrated).

Abstract:

A typical core is deeply embedded in the chip of a system so that direct access to its input/output is not possible. Built in self test (BIST) structures are excellent solutions for testing embedded cores.

In this work, an 8 ×8 modified Booth multiplier has been implemented with low power test pattern generators (TPG). Complete design was implemented using 0.25-micron technology. The BIST TPG architectures compared were: 8-bit binary counter, 8-bit gray counter and combination of gray and binary counter. Different TPGs have been compared in terms of average power dissipation, fault coverage. Reduction in power dissipation has been achieved by properly assigning the TPG outputs to the multiplier inputs, significantly reducing the test set length and suitable TPG built of a 4-bit binary and 4-bit gray counter. Experimental results show that combination of gray and binary counter can achieve power reduction from 21 %to 45% without affecting the quality of test. BIST architecture for modified Booth multiplier is proposed. Proposed architecture covers stuck at faults, stuck open faults and non-feedback bridging faults. It also provides fault coverage greater than 98 % for stuck-at faults, stuck-open faults and non-feedback faults.

2005-2007

Author: Agarwal, Vaibhav (200511037)
Title: ASIC Implementation of a Pipelined Bitrapezoidal Architecture For Discrete Covariance Kalman Filter; ix, 44 p.; 2007.
Supervisor: Dubey, Rahul
Call No.: 629.831222 AGA
Acc. No.: T00127
Keywords: Kalman filtering; Nonlinear systems; Mathematical optimization; Adaptive filters; Filters, digital electronic; ASIC.

Abstract: This work presents, the complete ASIC implementation of Discrete Covariance Kalman ¯lter, on a Parallel and Pipelined Bitrapezoidal Systolic Array architecture. The Kalman Filter equations are mapped on the designed architecture. This mapping requires, decomposing the overall equations, to calculate the Schur's complement, using Faddeev's algorithm. This facilitates an approach, to avoid the iterative process of calculation of matrix inverse. The designed Parallel and Pipelined architecture caters to high speed applications, by computing the single iteration of the filter in just 6 steps, each step individually taking only O(n) clock cycles. Further the processing efficiency is increased, by computing equations of O(n3) complexity in just O(n2) complexity only, where n is the order of the filter. Other unique feature of the designed architecture includes, increased robustness to rounding errors and resolving the reiterative Data input problem. The ASIC implementation was done by, Modelling the architecture using Verilog HDL,its Functional Verification was done, Logic Synthesis was done on Cadence RC 5:2 Synthesizer and Physical Synthesis on Cadence SOC Encounter. The implementation methodology presented for logic and physical synthesis resulted in efficient implementation of architecture in silicon. The design was mapped to target technology of 180nm and the synthesis results were analyzed. Physical synthesis was carried out for the same technology and the design gives final timing closure for 50MHz, which is quite high for a compute intensive algorithm like Kalman filter.

Author: Aggarwal, Divya (200511023)
Title: A Fault Diagnosis Algorithm for a Flash ADC using Oscillation Based Testing Technique; ix, 44 p.; 2007.
Supervisor: Parikh, Chetan D.
Call No.: 621.39814 AGG
Acc. No.: T00118
Keywords: Analog-to-digital converters -- Design and construction; Digital-to-analog converters -- Design and construction; Electronic circuit design; Oscillators.

Abstract: With the advent of system-on-a-chip (SoC) designs, the semiconductor industry wants to solve problems that constrain the coexistence of analog and digital cores on a single chip. The complexities of modern (SoC's), comprising of analog, digital and even Radio-Frequency (RF) blocks on a single chip, are surpassing all the previous limits. Merging so many different technologies poses new challenges, such as developing design and test methodologies capable of ensuring system performance and reliability for a reasonable design effort. Digital testing has developed in to a complete science in the last forty years, but analog and mixed-signal are still in its initial state. The lack of standard models and methodologies is worsening this situation.

This work addresses the problem of fault coverage in analog and mixed signal circuits and proposes a fault diagnosis algorithm using Oscillation based Testing Technique. Present calibration techniques compensate for deviations in the measured parameters and do not correct the faulty value, because the faulty value cannot be obtained. A fault diagnosis technique able to perform fault identification (obtain fault values) will lay the groundwork for the development of more effective calibration techniques. Analog to digital converter (ADC) is used as a test vehicle to demonstrate the capability of the proposed OBIST technique. This technique employ Oscillation

frequency test data for fault location and identification of the analog components in the converter. In the flash ADC, a fault causes deviation of Oscillation frequency from the ideal one. Hence, it can be considered as a functional signature of the ADC and this property is employed for fault diagnosis. ADC's are virtually in all modern SoC's and hence are one of the most important modules in analog and mixed-signal designs. Here, we have 3-bit, 1 GHz CMOS Flash ADC, designed in 0.18 µm CMOS technology as a benchmark. The simulation results prove that this technique shows an excellent coverage of catastrophic as well as a good coverage of parametric faults, also the algorithm proposed locate the faults in resistive ladder and comparators. The area overhead is very less in this techniques and it works on the circuit speed so, lesser test time.

Author: Bhatt, Vishal (200511016)
Title: Low Power Microprocessor Design; x, 79 p.; 2007.
Supervisor: Dubey, Rahul
Call No.: 621.3916 BHA
Acc. No.: T00115
Keywords: Microprocessors -- Design and construction; Energy conservation; Low voltage integrated circuits -- Design and construction; Computer architecture.

Abstract: This research work tries to reduce the power consumption of a processor with signal processing features. For low power design, focus is on developing 'Low power synthesizable Register File', as the initial study shows that there is potential for significant benefit by doing this. Two techniques are proposed and implemented in this work, (1) Compiler Driven Register Access (CDRA) (2) Register Windowing. Here, Register Windowing is an extension to an earlier technique called 'Register Isolation'. Benchmarks used for evaluating design in terms of power consumption and performance, simulate conditions encountered by the processor in control and DSP applications. After applying various low power techniques, average power reduction obtained across benchmarks is 1.5% and the maximum power reduction obtained is 2.6% when compared to Base Processor which is a customized version of MIPS architecture with signal processing capability.

Author: Chaurey, Vasudha (200511020)
Title: An Architecture Design for Preliminary ECG Analysis System Using New DFT Based Analysis Technique; ix, 54 p.; 2007.
Supervisor: Nagchaudhari, Dipankar
Call No.: 621.1207547 CHA
Acc. No.: T00116
Keywords: Electrocardiography; Signal processing; Electrocardiography -- Interpretation -- Data processing; ASIC; Discrete Fourier Transform.

Abstract: This thesis proposes a hardware architecture of an ASIC for a portable ECG analysis system. The device is meant to record and analyze ECG signals in real time so as to detect the presence of abnormalities. In order to achieve this, a totally new approach for the analysis of ECG signals using Discrete Fourier Transform (DFT) is developed as a part of the thesis. An important finding of the project, through experiments performed on real ECG data in MATLAB, is that the phases of first 8 DFT coefficients of beat-wise ECG signals give distinguishing patterns for normal and abnormal beats. With this idea of variable size DFT as the basis, a much simplified form of the technique with fixed 32 point DFT is derived without significantly disturbing the patterns so as to make it suitable for hardware implementation. The translation of the algorithm to hardware architecture has been done in a way so as to achieve optimization in terms of area as well as power by minimizing the number of computations. One of the important features of the proposed architecture is the synchronization of the complete system which processes an asynchronous signal, i.e. the ECG beats, in real time. The thesis gives the custom Register Transfer Level architecture for the processing block of the system, which is meant for selecting fixed number of samples from every beat and do a customized DFT phase computation for detecting abnormalities. The project proposes a very simple technique for the beat detection as a part of optimization. Since the incoming signal is much slower than the processing rate, the proposed architecture is designed with the flexibility of adding extra functionalities in the system other than ECG analysis which if possible can use the same processing hardware during the wait periods.

Author: Chudasma, Nrupen (200511011)
Title: Service Selection using WS-Agreement; ix, 54 p.; 2008.
Supervisor: Chaudhary, Sanjay
Call No.: 658.562 CHU
Acc. No.: T00144
Keywords: Service-level agreements; Customer services; Performance -- Measurement.

Abstract: The business requirements are dynamic in nature and identification of suitable busi- ness partners "on demand", who can satisfy a set of guarantees is a critical process. Selection of business partners is influenced by several parameters including maximizing profit, minimizing cost, reliability, credit history, etc. A business process can be decomposed into several tasks, possibly expressed as Web services implementing desired business functionalities. Each service offers a set of guarantees, each defining a Service Level Objective(SLO). Many service providers may provide the similar business functionality in the form of service with different SLOs. Thus it is necessary to select the service offered by service partner such that overall performance of the process is improved.

The thesis proposes architecture for solving selection of the best service provided by available service partners. To put across our approach, the thesis has taken examples from the Agro-Produce marketing System. By specifying requirements of the service in the form of multiple service level objectives (SLOs), selection of a service provider can be achieved based on the best or optimal matching of SLOs of service consumer and providers. A set of services, SLOs, and participating actors constitute a Service Level Agreement (SLA). In this work, WS-Agreement specification is used to specify the SLA. For flexible selection, role of semantic web concepts such as ontology and semantic rule language is discussed. The service partner must comply with the multiple criteria and preferences of a requester, Multi Criteria Decision Making (MCDM) methods is required in the service selection process.

Two scenarios for service selection from Agro-Produce market system are taken. One is single service selection where selection of sellers selling mangos are selected based on the best seller offered. Second one is related to service composition where more than two services need to be selected, such that overall process performance is improved. The scenario is from rice production process where selection of farmer, rice-miller, storage provider and transporter contribute to overall cost, quantity and quality of rice.

Author: Desai, Meghana (200221006)
Title: A Design methodology for architecting Application specific instruction set processor; vii, 51 p.; 2007.
Supervisor: Dubey, Rahul
Call No.: 621.392 DES
Acc. No.: T00130
Keywords: Microprocessors -- Design and construction; Energy conservation; Low voltage integrated circuits -- Design and construction; Computer architecture.

Abstract: Application Specific Instruction-set Processors (ASIP), also referred as extensible processors, represent the state-of-the-art microprocessor architecture. ASIPs are practically leading towards the realization of System-on-a-Chip (SoC) concept; as processor, customised for an application, can be easily integrated in a SoC as pre-designed and pre-verified soft RTL block. Most significant and challenging part for these flexible or programmable processors is the design methodology. The challenge lies in providing a simple configurable design space such that the outcome is optimised, efficient and customised application specific processor hardware, with very short design cycle time. The bottle neck for a processor is chiefly the data path design, as it has computational intensive functional units which add to the major portion of hardware area along with timing. In case of ASIP as well, data path modification is to be achieved as per the requirements. Current electronic design automation (EDA) tools are intelligent and if exploited well can actually help in providing various optimizations in the design. The implemented design approach is based on these aspects of selection of accurate data path elements along with distributed control path and exploiting the inbuilt functionality of EDA tools for generating user defined architecture. In this project a non-pipelined as well as five stage pipelined processor

fabrics are implemented with configurable parameters. A library of basic arithmetic functional units is created from which a component of desired characteristic is selected and integrated in the data path. Synthesis of modified processor core is performed with a set of constraints to achieve required trade off between area, power and timing. Multi-supply voltage feature of the synthesis tool is exploited to meet the timing closure of the generated processor core.

Author: Dubey, Divya (200511014)
Title: Design of Low Voltage High Performance, Wide Bandwidth Current Feedback Amplifier with Complementary Input Pair; ix, 93 p.; 2007.
Supervisor: Parikh, Chetan D.
Call No.: 621.39732 DUB
Acc. No.: T00142
Keywords: Low voltage integrated circuits--Design and construction; Low voltage systems; Operational amplifiers -- Design and construction; CMOS current conveyor; Complementary input pair; High performance wide bandwidth.

Abstract: This thesis presents the work done on the design of a low voltage high performance, wide bandwidth current feedback amplifier [CFA] with complementary input pair. The design is carried out in 1.8 V, 0.18 micron CMOS process. The design uses the cascaded voltage follower configuration that improves the bandwidth of the amplifier and to get almost rail-to-rail input swing capability, parallel NMOS and PMOS differential pairs are used with current addition.

Thus proposed current feedback amplifier combines the advantages of both the design. It provides wide bandwidth and simultaneously increases the input voltage range. It also provides low power consumption and high transimpedance.

Simulation results show that the closed loop bandwidth for unity gain noninverting configuration is 458 MHz and the input voltage range is from –0.8 to 0.35 V, for supply voltages ranging from +0.9 to –0.9 V. The amplifier performance is also evaluated to see the gain bandwidth independence effect. This CFA provides almost gain independent closed loop bandwidth, which depends on the value of feedback resistor.

Author: Gahlot, Jai (200511014)
Title: Security Analysis of Two Fair Exchange Protocols; ix, 97 p.; 2007.
Supervisor: Mathuria, Anish
Call No.: 005.8 GAH
Acc. No.: T00113
Keywords: Computer security; Computer networks -- Access control; Computer network protocols; Privacy, Right of electronic commerce -- Security measures; Security assessment; Security auditing.

Abstract: E-commerce applications enable two parties to exchange digital items electronically. It is critical for such applications that the underlying protocols ensure the fairness requirement: no honest participant should suffer any loss of significant value. It is important to verify that an e-commerce protocol satisfies its fairness goal. Formal methods such as model checking can be helpful in this regard. To this end, it is essential to develop a model of the protocol under realistic assumptions. Using the NetBill protocol as an example this work shows how improper modelling can lead to incorrect claims about the protocol. It also shows how a carefully developed formal model can be successfully used to discover previously unknown flaws in an existing protocol.

Author: Goyal, Shweta (200511001)
Title: Design and Development of an Ontology for an Agriculture Information System; viii, 74 p.; 2007.
Supervisor: Chaudhary, Sanjay
Call No.: 025.06631 GOY
Acc. No.: T00103
Keywords: Information storage and retrieval systems - Agriculture Science; Agriculture science -- India – Databases; Agriculture -- Research -- Information services; Information integration; Ontology application; Ontology; Ontologies (Information retrieval); Expert systems (Computer science);

Information resources management; Agriculture--Information services; Database design; Database management; Conceptual structures (Information theory); Knowledge representation (Information theory); Semantic networks (Information theory).

Abstract: Traditional sources of information like books, agricultural extension officer are unable to provide specific information required by a farmer. There is a need to build an ontology based agriculture information system which can provide scientific, relevant and contextual information about various aspects of crop production cycle.

The aim is to develop a domain dependent ontology that will cover various aspects of crop production cycle. AGROVOC vocabulary developed by Food and Agriculture Organization is used for indexing and retrieving data in agricultural information systems. In the proposed research work, AGROVOC is used as base vocabulary to develop the proposed ontology (AGRIont). The ontology is developed by using open source tool Prot´eg´e 3.2. The ontology developed serves as a building block to an agriculture information system that answers the farmer's queries in their own native language and helps them in making decisions about various aspects of crop production cycle.

In this work, stages of ontology development, structure of ontology developed, architecture, query flow and process of query formulation for the proposed system are discussed in detail. At the end, guidelines to build an ontology, conclusions and future work are given.

Author: Grandhi, Durga Ganesh (200511026)
Title: Identifying the Protein Coding Regions in DNA Using IIR Antinotch Filter; vii, 32 p.; 2007.
Supervisor: Chakka, Vijakumar
Call No.: 621.3822 GRA
Acc. No.: T00119
Keywords: Cellular signal transduction; Genetic regulation; Control theory; Gene Expression Regulation – physiology; Genomics; Models, Theoretical; Signal Transduction – genetics; Protein coding; DNA

Abstract: Genomic Signal Processing is an emerging interdisciplinary area. The problem of Identifying Protein Coding Regions in DNA is addressed using signal processing techniques in this work. DNA can be thought of a string formed from the alphabet set A = {A,C,G, T}. It is found that in protein coding regions the symbols have periodicity of 3 [Trifonov and Sussman, 1980], known as period-3 property. In genomic signal processing, this periodicity is used as a cue, to identify the protein coding regions using signal processing techniques like Discrete Fourier Transform (DFT) and Digital Filtering. This is possible only if the symbol sequences are mapped to numbers. In this thesis it is identified that the computational complexity of the filters employed for identifying the protein coding regions presented in the DNA, is directly related to the choice of mapping. A new lower dimensional mapping is also proposed which reduces the computational complexity by half, producing results nearly equal to those produced by a higher dimensional mapping.

Author: Gupta, Amit Kumar (200511039)
Title: CMOS Latched Comparator Design for Analog to Digital Converters; v, 32 p.; 2007.
Supervisor: Parikh, Chetan D.
Call No.: 621.39732 GUP
Acc. No.: T00128
Keywords: Analog-to-digital converters; Digital-to-analog converters; CMOS (Electronics); Microwave integrated circuits--Design and construction; Microwave equipment Circuits; Complementary metal oxide semiconductor; CMOS (Metal oxide semiconductor, Complementary); Linear integrated circuits.

Abstract: Conventional comparators are at the two extremes as far as power delay product and isolation between input and output is concern. Either they achieved very good isolation at the cost of power in the preamplifier or save the static power dissipation in preamplifier in the latching mode which increases the feed through. In this thesis work we propose an optimized CMOS Latch Comparator. The simulation result based on .18um technology, shows the working of the comparator at 500 MHz, with moderate power delay product and isolation compared with the conventional architecture.

Author: Gupta, Mukesh (200511040)
Title: CMOS RFIC Mixer Design; xv, 128 p.; 2007.
Supervisor: Gupta, Sanjeev
Call No.: 621.39732 GUP
Acc. No.: T00129
Keywords: CMOS (Electronics); Microwave integrated circuits--Design and construction; Microwave equipment Circuits; Complementary metal oxide semiconductor; CMOS (Metal oxide semiconductor, Complementary); Linear integrated circuits -- Design and construction; Electronic circuit design.

Abstract: A CMOS RF (Radio Frequency) up/down conversion mixer results in a reasonable increase in transceiver integration and a reduction in cost. The design of mixers faces many compromises between conversion gain(GC), local oscillator (LO) power, linearity, noise figure (NF), port-to-port isolation, voltage scaling and power consumption. Mixer linearity is a very important parameter in transceiver design, because system linearity is often limited by the first down-conversion mixer due to a relatively large signal compared with that at the LNA input. Since active FET (Field Effect Transistor) mixers achieve conversion gain with lower LO power than their passive counterparts, the active CMOS single-balanced and double-balanced Gilbert mixers are commonly used in the CMOS transceiver design. Compared with the single-balanced counterpart, the double balanced mixer has better port-to- port isolation due to symmetrical architecture. The double-balanced mixer has a higher noise figure due to more noise generators. The overall Gilbert mixer linearity is controlled primarily by the transconductance stage if the LO-driven transistors act as good switches.

This report describes a Gilbert cell mixer with source degeneration for 900 MHz frequency. The circuit converts a 900 MHz RF signal directly to base band [IF (Intermediate frequency) 45 MHz] using an 855 MHz LO frequency. The mixer uses common source MOSFETs with inductive degeneration to convert the input RF voltage to a current. This current is then steered using a switching network composed of MOSFETs that is driven with the LO and a 180 degree phase-shifted version of the LO. Gilbert Mixer achieves gain through an active predriver [The V-I (voltage to current) converter]. This V-I converter is highly nonlinear; hence, the Gilbert Mixer distortion performance is worse. This thesis tries to propose a simple linearity improvement technique for Gilbert Cell Mixer by including an additional capacitor located in parallel with the intrinsic gate-source capacitor of the common source transconductance stage. Also, to reduce the flicker noise of the switching transistors which depends on the frequency and circuit capacitance at the common source node of the switching stage, a method is used to reduce this capacitance by adding an extra inductor that helps for simultaneously match low 1/f noise, high linearity and low NF at the expense of Conversion gain. The design is based upon the third order intermodulation distortion (IM3) and output current equations of MOSFETs and flicker noise equation when it is subjected to an ac input signal. The performance has been verified using Agilent' Advanced Design System (ADS) simulations. The designed mixer has a voltage conversion gain of 15.804 dB, NFSSB of 6.565 dB, NFDSB=3.975 dB, IIP3 of -1.158 dBm, OIP3 USB of 14.699 dBm, OIP3 LSB of 14.646 dBm, LO to IF isolation of -27.532 dB, LO to RF isolation of -69.365 dB and RF to IF isolation of -56.554 dB for single ended RF Input.

Author: Gupta, Navneet (200511028)
Title: ASIC Implementation of Discrete Fourier Transform Processing Module; iv, 54 p.; 2007.
Supervisor: Dubey, Rahul
Call No.: 621.3815 GUP
Acc. No.: T00121
Keywords: Fourier – introduction; Fourier transformations--Data processing; Fourier analysis--Data processing; Laplace transformation; Fourier series; Discrete fourier transform; Fourier Transforms; DFT and FFT Processing; Integrated circuits; ASIC; Application specific integrated circuits -- Design and construction; Application specific integrated circuits.

Abstract: This work presents the design and ASIC implementation of Discrete Fourier Transform Processing Module. The performance of designed DFT processing module is better than radix-2 and radix-4

FFT algorithms, and is comparable to Split radix FFT algorithm, in terms of computational requirements. Different architectures are proposed for DFT processing module, and their comparative analysis is done. ASIC implementation of Discrete Fourier Transform processing module includes, its modelling using Verilog HDL, gate level synthesis of the modelled design and physical synthesis of netlist generated by gate level synthesis. The functionality of Design after physical synthesis is verified. Designed DFT processing module is retargetable and can be used as an IP.

Author: Jain, Shubham (200511018)
Title: Localization for A Habitat Monitoring Sensor Network for Ground Turtles; viii, 109 p.; 2007.
Supervisor: Ranjan, Prabhat
Call No.: 681.2 JAI
Acc. No.: T00143
Keywords: Sensor networks; Algorithms; Coding theory; Computer network protocols; Databases and data processing; Localization; Ground turtles.

Abstract: This thesis work deals with the localization problem (i.e. finding the location of the sensor nodes) in sensor networks. This work is specifically concerned with the localization of the sensor nodes on small ground turtles in the campus of Wildlife Institute of India (WII), Dehradun, India. The location information about the turtle node will be helpful to the scientists at WII to conserve the turtles. The wildlife scientists are interested in knowing the places where turtles go, what food they eat and the temperature and humidity of the place where they hibernate. The primary purpose of the sensor network deployment is habitat monitoring and not location determination. The energy constraint which sensor networks usually have is partly removed by deploying a grid of fixed nodes which have electric supply. But the nodes on turtles have this constraint and the lifetime of the nodes on turtles can be roughly one year. There is a weight constraint. The weight of the node on turtles cannot be more than 25 gms. This constraint restricts the measurement technique that can be used for the localization. So Received Signal Strength or range-free localization will be used. The location information cannot be just 2D as the terrain in the WII campus is not flat surface but has highs and lows. So 3D location information will be available through the algorithm. Also, the network is not static as the turtles move although with a slow speed of about 10 cm/s. The accuracy of the location can be 10 m as the primary motive of this application is to find where the turtles go for eating food. This thesis report does not contain implementation details about the project although some details about the prototype network to be deployed are given. Also, there is a comparison of two localization algorithms that can be used for the implementation.

Author: Mangal, Anupam (200511003)
Title: On Path Complexities of Heapsort algorithm and the class Stack; ix, 49 p.; 2007.
Supervisor: Amin, Ashok T.
Call No.: 515.9 MAN
Acc. No.: T00105
Keywords: Complexity Theory; Computational complexity; Algorithms; Paths and cycles (Graph theory); Graph Theory; Path analysis; Heapsort.

Abstract: A measure of program complexity, called Path Complexity, based on the number of program execution paths as a function of the input size n, is proposed in [AJ05]. This measure can be used to compare the complexity of two different programs even with isomorphic control flow graphs. Using this measure, we determine the path complexity of the Heapsort algorithm. The notion of path complexity of a program is further extended to introduce the path complexity of a class. In particular, the path complexity of the Stack class is determined. We also provide an upper bound, and a lower bound based on catalan numbers, on the path complexity of the Stack class.

Author: Mehta, Janki (200511029)
Title: Check pointing and Recovery Mechanism in Grid; viii, 57 p.; 2007.
Supervisor: Chaudhary, Sanjay

Call No.: 004.36 MEH

Acc. No.: T00122

Keywords: Computational grids (Computer systems); Globus (Electronic resource); Application software—Development; Grid computing; Grid architectures; Grid middleware and toolkits; Computer software--Development.

Abstract: Grid is a collection of distributed computing resources that performs tasks in co-ordination to achieve high-end computational capabilities. Grid Computing is a collective computing of a given task by breaking it into sub-tasks. Each sub-task could be large and run for several hours or days on a number of grid nodes. If a sub-task fails to complete even on a single site, all the computations need to be done again. In scalable distributed systems, individual component failures usually does not result in failure of the entire system. However, a single failure may crash an entire parallel application. Grid is dynamic in nature. Since the probability of a single component failure rises rapidly with the number of components in the system, as system grows in size, efficient recovery mechanism is most important for highly parallel mission critical and long running applications of grid environment.

This thesis addresses a recovery mechanism using checkpoints to recover from Grid Service failure resulting in task or transaction failure in Computational Grid and Data Grid which will prevent computations to be restarted from scratch. Grid Service may fail as a result of hardware or software fault. A checkpoint is a point in time snapshot of a grid node in which its state information is stored. It will help in reducing the crash recovery time.

This work helps in preserving two main objectives of grid namely optimal resource utilization and speedy computations which can be achieved by using resources in a better way for improving performance of system rather than engaging them in tasks like rollbacks resulting from cascading aborts. The saved state using checkpoints can also be used for job migration using job schedulers of grid on occurrence of critical failures like Operating System failure. Experiments conducted provide integration of proposed mechanism with standard grid Web Service Resource Framework and will aid in future development work.

Author: Mistry, Kamal (200511005)

Title: Buffer Aware Routing in Interplanetary Ad Hoc Network; x, 70 p.; 2007.

Supervisor: Srivastava, Sanjay and Lenin, R B (Co-supervisor)

Call No.: 621.38216 MIS

Acc. No.: T00107

Keywords: Routers (Computer networks); TCP/IP (Computer network protocol); Computer network protocols. Asynchronous transfer mode; Telecommunication -- Switching systems.

Abstract: Recent research has shown that existing TCP/IP protocol suit exhibits poor performance in space communication networks. To deal with communication challenges in deep space such as long propagation delay, high channel error rate, limited bandwidth etc. the architecture called Interplanetary Ad hoc Network (IPAN) is envisioned to establish a communication infrastructure in environment which allows to connect planets, natural and artificial satellites, and various mission elements such as space- crafts and rovers. The communication links in IPANs possess the properties of low bandwidth, high error rate, high latency and link unavailability for longer period of time. Nodes in such networks are resource constrained in terms of storage, energy and processing power. This work proposes a probabilistic routing protocol called \Buffer Aware Routing Protocol in Interplanetary Ad hoc Network (BARPIN)" based on the store and forward principle of Delay Tolerant Networking (DTN). Here IPAN is modeled as the network of two kinds of nodes, one having deterministic mobility patterns with greater resources and the others having random movement patterns with limited resources in terms of storage and energy. The delivery ratio performance measure of BARPIN is studied for different network conditions by changing field sizes, traffic rates, available resources on various nodes and for different source-destination pairs. Further we propose a model to estimate the minimum required buffer size of nodes for different data rates to reduce the packet loss due to buffer overflow, and justified the simulation results with analytical results.

Author: Munjal, Aarti (200511002)

Title: Modeling MANETs Using Queuing Networks; viii, 48 p.; 2007.
Supervisor: Srivastava, Sanjay and Lenin, R B
Call No.: 621.38456 MUN
Acc. No.: T00104
Keywords: Cellular telephones; Cellular telephone systems; Cellular telephone systems--Technological innovations; Cellular telephone systems--Design and construction; Mobile computing; Mobile communication systems; Mobile ad hoc networks; Wireless communication systems; Computer networks; Routers (Computer networks); Wireless LANs; Queuing theory.

Abstract: Mobile Ad Hoc Networks (MANETs) are becoming an attractive solution to the services that require flexible establishment, dynamic and low cost wireless connectivity. Since nodes are mobile, routing results vary significantly with the underlying mobility model. So, modeling (nodes as well as wireless links between them) plays a critical role in the performance analysis of MANETs. This work involves modeling MANETs in two ways. In the first model, nodes are modeled as static and wireless links between a pair of nodes are available or unavailable for exponential durations. When the link is available, nodes are connected and can have data transmission and data are lost if the link is not available as the nodes are not connected. Second model involves mobility being captured by making the servers go ON/OFF for exponential amount of time, and no departure takes place while server is on vacation. This way one does not lose packets but the queuing delay increases. In this work, these two queuing networks are proposed to study to performance measures of MANETs. Numerical results are derived using mathematical equations and then verified through simulation.

Author: Nimmagadda, Rahul (200511033)
Title: Identifying Mutant Hierarchies to Reduce Test Effort in Mutation Testing; ix, 73 p.; 2007.
Supervisor: Kapoor, Kalpesh
Call No.: 005.14 NIM
Acc. No.: T00125
Keywords: Computer software – Testing; Testing techniques; Operation acceptance testing; Mutation testing Fault based testing.

Abstract: Mutation testing is a fault-based testing approach. The main goal of mutation testing is to assess the quality of a test suite, and in that process, test the software. The approach asserts the absence of pre-specified faults. In mutation testing, a single syntactic change is made and the resulting program is referred to as 'Mutant'. The mutants obtained by making n syntactic changes are known as nth-order mutants'. Mutation Testing is based on two hypotheses, (i) Coupling Hypothesis assumes if a test suite can detect a first-order mutant from the original program, it will detect most higher-order mutants, (ii) Competent Programmer Hypothesis assumes the program to be tested is "close" to the intended program. Mutation testing is practically infeasible because the number of generated mutants is myriad for each program. It is also resource intensive requiring substantial amount of computation power and time to execute all the mutants against the original program for a given test suite.

The objective of this thesis is two-fold. First, an empirical study is done to validate a formal approach proposed [Kapoor, K and Bowen, J. P, 2004] to reduce the test effort required in mutation testing. The formal approach orders the mutants in a hierarchy such that a mutant occurring higher in the hierarchy is stronger than a mutant occurring lower in the hierarchy. If a test suite can distinguish the original program from a stronger mutant, it is guaranteed to distinguish any mutant occurring lower than the stronger mutant in the hierarchy. Second, the concept of conditional strong mutant for relational operators is proposed which is a specialisation of the strong mutant concept. It further reduces the test effort by identifying more number of strong mutants through some constraints on the operands of the relational operators.

The savings obtained by using conditional strong mutants is more than that obtained by strong mutants. There is a saving of 80% in the test effort required involving mutants generated by invoking the Relational Operator Replacement (ROR) operator on conditions present in the branch statements of a program. The analysis done applies to any program containing relational operators in the conditions of branch statements.

Author: Nayudu, Bharath Kumar (200511027)
Title: Design of CMOS Voltage Controlled Oscillator for High Tuning Range; xii, 67 p.; 2007.
Supervisor: Gupta, Sanjeev
Call No.: 621.39732 NAY
Acc. No.: T00120
Keywords: Metal oxide semiconductors, Complementary; Oscillators; Oscillators, Electric; Oscillators, Electric--Design and construction; CMOS.

Abstract: The main objective of the work is to design a CMOS voltage controlled oscillator for higher tuning range. Today there is a great need for multi-standard wireless receivers in the wireless communications. A receiver is to be designed such that it receives data from the different frequency bands and standards. It is essential to design an oscillator to adhere to some of the standards like CDMA, GSM, GPRS and others. CMOS was the ideal choice for this work because of its low power consumption compared to other technologies and its immunity to the noise. In the design of the tank circuit, binary weighted capacitive array technique (BWCA), discrete variable inductor by using MOS switch and variable capacitor for continuous tuning have been used. By using all the above three techniques, a higher tuning range has been achieved.

Author: Paluri, Santosh Kumar (200511015)
Title: Web Content Outlier Detection Using Latent Semantic Indexing; vii, 36 p.; 2007.
Supervisor: Jotwani, Naresh
Call No.: 006.312 PAL
Acc. No.: T00114
Keywords: Outliers (Statistics); Content analysis (Communication); Data mining; Web sites; Web databases; Semantics; Semantics of Data; Semantic Database Models.

Abstract: Outliers are data elements different from the other elements in the category from which they are mined. Finding outliers in web data is considered as web outlier mining. This thesis explores web content outlier mining which finds applications in electronic commerce, finding novelty in text, etc. Web content outliers are text documents having varying contents from the rest of the documents taken from the same domain. Existing approaches for this problem uses lexical match techniques such as n-grams which are prone to problems like synonymy (expressing the same word in different ways), which leads to poor recall (an important measure for evaluating a search strategy). In this thesis we use Latent Semantic Indexing (LSI) to represent the documents and terms as vectors in a reduced dimensional space and thereby separating the outlying documents

from the rest of the corpus. Experimental results using embedded outliers in chapter four indicate the proposed idea is successful and also better than the existing approaches to mine web content outliers.

Author: Parashar, Umesh (200511004)
Title: Low Power Improved Full Scan BIST; ix, 66 p.; 2007.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.3950287 PAR
Acc. No.: T00106
Keywords: Embedded computer systems – Testing; Computer firmware; Electronic apparatus and appliances – Testing; Electronic apparatus and appliances -- Design and construction; Very large scale integration (VLSI); Automatic checkout equipment; Integrated circuits – Testing; Built-in self-test.

Abstract: Low power testing of VLSI circuits has recently become an area of concern due to yield and reliability problems. Past research on low power testing has shown that, switching activity and test time are the main factors that influence the heat dissipation during test. This thesis presents a scan-based BIST scheme that reduces switching activity (SA) in the circuit under test (CUT) and test application time without compromising in fault coverage (FC).

The proposed BIST scheme is based on combined BIST approach (combining both test-per-scan and test-per-clock test methodologies), two different functional lengths during scan, and a low transition random test pattern generator (LT-RTPG) as TPG. It takes optimal advantage of three techniques and reaches desired FC faster with a significant reduction in switching activity.

Experiments conducted on different ISCAS'89 benchmark circuits report up to 24% reduction in SA and up to 80% reduction in the test length.

The register transfer level (RTL) implementation of the proposed BIST is done on a 4-bit sequential multiplier circuit (for 90nm technology; Spartan-3 FPGA) to validate effectiveness of the proposed BIST under constraints of supply voltage, glitches, and technology parameters (for 90nm). Experimental results show that proposed BIST achieves 13.75% reduction in the average power dissipation compared to LFSR based BIST

Author: Patel, Animesh (200511006)
Title: Channel Quality Prediction And Localization; viii, 47 p.; 2007.
Supervisor: Jotwani, Naresh
Call No.: 621.38411 PAT
Acc. No.: T00108
Keywords: Wireless communication systems -- Security measures; Wireless communication systems; Wireless LANs; Radio communication; Wave propagation and transmission.

Abstract: In this thesis we focus on two problems, Channel Quality Prediction and Localization in wireless network. In High-Speed Downlink Packet Access (HSDPA) architecture of Universal Mobile Telecommunications Services (UMTS), User Equipment (UE) provides Channel Quality Indicator (CQI) values to Node B (base station), as an indication of current channel quality. We investigate two methods for channel quality prediction, which can be implemented at Node B. Each of these methods uses recent CQI values to predict future channel quality, i.e. future CQI values. Experiments are conducted in different environments, to check accuracy of these methods and found that the simple method using Least-Squares Line gives as good results as the complex method using Spline. Packet schedulers can be developed which uses predicted CQI values for scheduling. Cellular networks are used for localization where the UEs are located by measuring the signal traveling to and from a set of fixed cellular base stations (Node B). We propose a Markov Chain Model, which can be used as supplement to Angle of Arrival (AOA) method which is used for localization. Sector-specific information with recent CQI values and information about angle of arrival of signal can be used to estimate UE's location using proposed model, in UMTS network supporting HSDPA architecture.

Author: Patidar, Pravin (200511032)
Title: A Model Based Channel Shortening Technique For IEEE 802.11a OFDM System; ix, 54 p.; 2007.
Supervisor: Chakka, Vijaykumar
Call No.: 621.3821 PAT
Acc. No.: T00124
Keywords: Wireless communication systems – Standards; Mobile communication systems; IEEE 802.11 (Standard); OFDM (Orthogonal Frequency Division Multiplexing).

Abstract: Channel shortening tehniques for IEEE802.11a OFDM system are studied. Their performance is evaluated for various standard channel models. A model based channel shortening technique is presented, which reduces the computational comlexity, both during initialization and data transmission. The method is based on modeling of channel impulse response by a pole-zero system, and using the denominator coefficients as the equalizer. Further, it is shown that for channel shortening, calculation of zeros of the model is not required. Comparison of proposed technique with MMSE and MSSNR channel shortening techniques is presented.

Author: Pradhan, Pratik (200511008)
Title: A Packet Scheduling Algorithm to Improve Delay Bounds in HSDPA; viii, 79 p.; 2007.
Supervisor: Jotwani, Naresh
Call No.: 621.3845 GAH
Acc. No.: T00110
Keywords: UMTS; Multimedia Telephony; Data Transfer Technique; Wireless communications networks; Telecommunication--Traffic—Management; Asynchronous transfer mode; HSDPA.

Abstract: With tremendous growth in mobile subscribers in recent past and trend of accessing packet data services in wireless networks, 3GPP has introduced an enhancement to Universal Mobile Telecommunications System (UMTS) standard known as High Speed Downlink Packet Access (HSDPA) to provide high data rate services, especially in the downlink. The main focus of HSDPA concept is to increase peak data rates, improve Quality of Service (QoS) and enhance the spectral efficiency for downlink packet data traffic.

HSDPA introduces new transport channel named High Speed-Downlink Shared Channel (HS-DSCH) in downlink that is shared among the users accessing packet data services. Scheduling of these users is one of the most challenging and interesting problem because of constantly varying state of the wireless channel. The problem is even worse when users require certain level of QoS and the transmission rate supported by wireless channel is also varying.

The Exponential Scheduling Algorithm, proposed in literature, is a good candidate to provide bounded delays when QoS requirements are speci¯ed in terms of maximum tolerable delays, but the investigations in this thesis show that it fails to provide delay bounds when it is still possible with some trade-o® with system throughput and sometimes not even that.

The thesis proposes Delay Sense-Exponential Scheduling Algorithm, a variant of Exponential Scheduling Algorithm, to improve on the delay bounds provided by Exponential algorithm. The simulation results ensure that the new proposed algorithm improves on providing delay bounds to the Real Time (RT) services simultaneously providing comparable throughput to Non-Real Time (NRT) services. The proposed algorithm is studied under wide range of scenarios including NRT, RT and mixture of NRT and RT services.

Author: Praveen, Asim Rama (200511007)
Title: A Study of Algebraic and State based Testing Techniques; vii, 47 p.; 2007.
Supervisor: Kapoor, Kalpesh
Call No.: 005.14 ASI
Acc. No.: T00109
Keywords: Computer software—Testing; Testing Techniques; Operations Acceptance Testing; Computer programs—testing; Computer programs--Testing--Data processing; Algebraic based testing technique; State based testing technique.

Abstract: Sequential programs can be modeled as algebra or transitions on a state space. Whether a program is implemented according to its model is the question addressed by program testing. The thesis illustrates issues in constructing a finite test set from algebraic and state transition based specifications. Test hypotheses need to be formulated to generalise results of testing from a finite test set to the entire input domain of a program under test. It is demonstrated with examples that test hypotheses are constraints on program under test. Testing can lead to sound conclusions for the class of programs that satisfy the constraints. The theory proposed in [BGM91] is used to illustrate test selection from algebraic specifications. Z notation is used to express state transitions of a heap sort example that illustrates testing from state based specifications.

Author: Raju, K. (200511035)
Title: Frequency Compensation Technique For Low Voltage Three Stage Operational Amplifier; ix, 54 p.; 2007.
Supervisor: Parikh, Chetan D.
Call No.: 621.395 RAJ
Acc. No.: T00126
Keywords: Operational amplifiers; Feedback (Electronics); Low voltage integrated circuits.

Abstract: This thesis presents a new frequency compensation technique for low supply voltage three-stage operational amplifier at higher loads. It is based on the miller splitting and pole-zero cancellation using feed-forward path. To reduce the value of compensation capacitance feedback stage is added in series with the compensation capacitance. The amplifier exhibits a dc gain 72db,a gain bandwidth of 35MHz at 63 degree phase margin slew rate 1 v/sμ, a compensation capacitance 4.5pF and load capacitance 300pF while consuming 395Wμat a 1-V supply voltage.

Author: Ravisankar, K. (200511013)
Title: An Investigation of Low Power Design of Left-Right Leap Frog Array Multiplier; ix, 56 p.; 2007.
Supervisor: Nagchaudhari, Dipankar
Call No.: 621.395 RAV
Acc. No.: T00112
Keywords: Low voltage integrated circuits; Low voltage integrated circuits--Design and construction; Low voltage systems--Design and construction; Linear integrated circuits--Design and construction; Linear integrated circuits; Electronic circuit design.

Abstract: This thesis addresses the Low Power design of 12 bit LRLFAM at the Layout, circuit and logic levels. A new Low power Booth-Recoder (BR), and Multiplexer based partial product generated are designed using pass-Transistor logic. Several 1-Bit full adders are studied: Transmission gate, 10T, 14T, 16T, Multiplexer based and 22T. Experiments show that all these adders produce glitches when used in LRLFAM. A 22T adder is designed that best suits the LRLFA architecture. Floor planning is done with minimum interconnect length has primary aim. LRLFA architecture presented in the literature is modified to reduce the glitches and delay by adding sign extension bits in later stages than in the first row. All the layouts are done using MAGIC 7.1 for TSMC 0.25u technology. Simulations are done using L.T Spice.

Author: Sharma, Adarsh (200511024)
Title: Mining Effective Association Rules Using Support-Conviction Framework; vi, 37 p.; 2007.
Supervisor: Jotwani, Naresh
Call No.: 006.312 SHA
Acc. No.: T00131
Keywords: Data mining -- Quality control; Data mining and algorithms; Data mining—Applications; Data mining; Support-conviction.

Abstract: Discovering association rules is one of the most important tasks in data mining. Most of the research has been done on association rule mining by using the support-confidence framework. In this thesis, we point out some drawbacks of the support-confidence framework for mining association rules. In order to avoid the limitations in the rule selection criterion, we replace confidence by the conviction, which is a more reliable measure of implication rules. We have generated the test data synthetically by the Hierarchical Synthetic Data Generator, which appropriately models the customer behaviour in the retailing environment. Experimental Results show that there is higher correlation between the antecedent and consequent of the rules produced by the supportconviction framework compared with the rules produced by support-confidence framework. Although support-conviction framework mines the effective associations but the association rules generated are large in numbers that are difficult to deal with. To overcome this problem, we propose an association rule pruning algorithm, which produces non-redundant and significant rules. Results obtained with synthetic data show that the proposed approach for mining association rules is quite effective and generates meaningful associations among the sets of data items.

Author: Sharma, Swati (200511009)
Title: Practical Approaches for Photometric Stereo; ix, 59 p.; 2007.
Supervisor: Joshi, M. V.
Call No.: 621.321 SHA
Acc. No.: T00111
Keywords: Computer vision; Image reconstruction; Image Restoration; Photometric.

Abstract: In this thesis work, we aim to propose approaches for photometric stereo that are less time consuming and have low computational requirements. Many applications of computer vision require high resolution 3-D structure of the object and high resolution image in order to take better decisions. However, in practical scenario, the major requirement is to obtain these within the time limit specified by the application. In this thesis, we first consider the problem of estimating the high resolution surface gradients, albedo and the intensity field using photometric stereo. Assuming a Lambertian model, the surface gradients and the albedo are estimated using

Least Square (LS), Constrained Least Square (CLS) and Total Least Square (TLS) approaches. High resolution depth map as well as image is then obtained using generalized interpolation. These methods are computationally less taxing and hence fast. A comparison of these methods with a regularization based approach is presented, which is computationally very expensive.

We also propose a simple approach for estimating the light source position (which is generally assumed to be known) from a single image. The proposed method is based on the shading information in the images and does not require any calibration.

Next we formulate a suitable regularization scheme for simultaneously estimating light source position, surface gradients and albedo given a number of images of a stationary object captured from a stationary camera by changing the light source position. The optimization is carried out using simulated annealing and graph cuts minimization techniques, to get better estimates for the illuminant position, surface gradients and albedo. Although simulated annealing guarantees global minima for any arbitrary energy function, it takes hours for convergence. This makes it inappropriate in practical situations. So, we also look into the use of graph cuts minimization method which converges very fast. We present a comparison of the performance of simulated annealing and graph cuts optimization methods.

Our first approach for obtaining high resolution depth and image using LS, CLS and TLS minimization methods with generalized interpolation, does not use any regularization which becomes essential while estimating high resolution image intensities and depth values, which is an ill-posed problem. Finally, we estimate the superresolved image and depth map using photometric cue and graph cuts optimization using a discontinuity preserving prior. Our results show that the high resolution images reconstructed using our approach that uses graph cuts minimization are much superior as compared to the approaches that use general interpolation methods.

Author: Singhal, Deepti (200511030)
Title: A Fair Downlink Packet Scheduling Approach to Support QoS in HSDPA Environment; ix, 69 p.; 2007.
Supervisor: Jotwani, Naresh
Call No.: 621.3845 SIN
Acc. No.: T00123
Keywords: UMTS; Multimedia Telephony; Data transfer technique; Wireless communications networks; Telecommunication--Traffic—Management; Asynchronous transfer mode.

Abstract: Traditionally, only best-effort traffic is supported by packet switching networks, but newer applications need communication services that allow end client to transport data with performance guarantees given in terms of data transfer reliability, available bandwidth and delay bounds. The choice of the packet-scheduling algorithm to be used at switching nodes is very crucial to provide the Quality of Service, QoS.

This work aims at designing a downlink packet scheduling approach to QoS provisioning in High Speed Downlink Packet Access, HSDPA, based UMTS networks. In UMTS a single logical channel is shared among multiple contending users. Besides better link utilization, scheduling disciplines seek to achieve fair allocation of this shared resource. However, these two criterions can potentially be in conflict. In this work a scheduling discipline, \Wireless Fair - High Speed Scheduling", is proposed, which addresses the above-mentioned conflict. The idea is to allocate the channel fairly among users, even during short time scales, according to their data rate requirements.

The proposed algorithm is compared with Adaptive Proportional Fair Algorithm, which provides fair distribution of channel bandwidth, proportional to the data rate requirements of users. Several experiments were conducted using simulation for comparing the performance of the algorithms in different scenarios. The results ensure that the proposed scheduling algorithm provides better link utilization, and long-term and short-term fairness among users even in heavy load conditions.

Author: Upraity, Maitry (200511022)
Title: Area Reduction in 8 Bit Binary DAC using Current Multiplication; ix, 68 p.; 2007.
Supervisor: Parikh, Chetan D.

Call No.: 621.39814 UPR
Acc. No.: T00117
Keywords: Analog-to-digital converters -- Design and construction; Digital-to-analog converters -- Design and construction; Electronic circuit design; Microwave integrated circuits -- Design and construction; Linear integrated circuits; Microwave equipment circuits.

Abstract: A proposed current multiplication technique is applied on 8 bit binary current steering Digital-to - Analog Converters with LSB 150 µA, to reduce area. MSB 1 and MSB 2 current are first kept half to reduce area and then current multiplication is performed to get the desired output.

Compare to the conventional binary current steering Digital-to-Analog Converters, 20.66% area is reduced and static errors are found within limit. Maximum Integral nonlinearity is-18µA (< LSB) and Differential nonlinearity5.02 µA (< LSB).

2006-2008

Author: Agarwal, Chetan (200611036)
Title: Use of Probabilistic Context Free Grammar For Natural Language Interface For An Application; ix, 47 p.; 2008.
Supervisor: Jotwani, Naresh D.
Call No.: 006.35 AGA
Acc. No.: T00183
Keywords: Human-computer interaction; User interfaces (Computer systems); Natural language processing (Computer science); Information retrieval; Interactive computer systems.

Abstract: This thesis report deals with the development of a natural language interface for a database application (library system). This application uses Probabilistic Context Free Grammar as a computation model. The material presented in this thesis provides an overview to study the topics on Natural Language Processing, Probabilistic Context Free Grammar, Parsing and extracting the semantic from a pare tree.

Probabilistic Context Free Grammar is a computational model which defines probabilistic relationships among a set of production rules for a given grammar. These probabilistic relationships among production rules have several advantages in natural language processing. The goal of natural language processing is to build computational models of Natural Languages for its analysis and generation. Application build takes a simple English sentence, parses the sentence, extracts the semantic and translates it into an SQL query. Application (library system) is coded in programming language JAVA. Though the given code is for a simple library system but can be modified according to requirements fulfilling the criteria of targeted task.

Author: Arya, Krishna (200611004)
Title: Multirate Signal Processing in Digital Communication; xii, 98 p.; 2008.
Supervisor: Chakka, Vijaykumar
Call No.: 621.3822 ARY
Acc. No.: T00148
Keywords: Signal processing -- Digital techniques; Signal processing -- Digital techniques – Mathematics; OFDM

Abstract: Fundamentals of multirate signal processing and perfect reconstruction filter banks are revisited. An attempt is made to develop a good understanding of concepts by connecting the filter bank design issues to the concepts of linear algebra. An interpretation of multicarrier systems in the form of transmultiplexers is provided and the notion of resampling of channel is introduced. A pulse shaping filter for the OFDM systems is proposed to remove the constraint of Cyclic Prefix. A comparison of performance of OFDM and filter bank based multicarrier systems in terms of stop band attenuation is provided. Notion of MIMO biorthogonal partners and the conditions for existence of FIR biorthogonal partners are studied. Emphasis is put on finding out the Greatest Right Common Divisor (GRCD) of polynomial matrices.

Author: Bajaj, Garima (200611009)
Title: Adaptive Biased Switched Capacitor Filters; ix, 51 p.; 2008.
Supervisor: Parikh, Chetan D.
Call No.: 621.3815324 BAJ
Acc. No.: T00152
Keywords: Switched capacitor circuits; Low voltage integrated circuits; Switched capacitor filters; Metal oxide semiconductors; Integrated circuits.

Abstract: The demand from today's handheld devices, such as laptop, ipod, cellphones is to have a long

battery life with no compromises in speed. The devices dissipate power even in standby mode also. Op-amp is a major block in all these devices. Its application in these devices may be as an amplifier, filter, A/D or D/A convertor. In most of the cases the op-amp may be in standby mode with no input signal. Power dissipated in these standby periods is wasted, and this is of concern for two reasons. First, in battery powered equipment, supply power must be conserved to extend the battery life. Second, any power wasted in the circuit is dissipated in the active devices which mean that they operate at higher temperatures and thus have a greater chance of failure. So the point of major concern is to reduce power in standby modes, and to give high speed when the device is operating.

This research work makes an attempt to design the most common application of Op-amp, a filter, such that it consumes low power with no compromise in speed. It ensures that the load capacitor of op-amp settles to the final value at a much faster speed, and at the same time consuming less power in stand by mode. The filter is designed for a cut off frequency of 100KHz at 2.5V in 0.18µm technology. The filter with a higher cut off frequency requires higher current and thus results in large power dissipation. The two Op-amps discussed, are proved and verified that they consume very less power for such a high cut off frequency.

Author: Bambhaniya, Prashant (200611043)
Title: Low Power SRAM Design; ix, 62 p.; 2008.
Supervisor: Dubey, Rahul
Call No.: 621.3973 BAM
Acc. No.: T00173
Keywords: Random access memory – Design; Random access memory; Electronic circuit design; Semiconductor storage devices; Microprocessors; Application specific integrated circuits; Integrated circuits -- Very large scale integration; Computer storage devices – Testing; Semiconductor storage devices -- Testing.

Abstract: In the past, power dissipation was not constraining factor because of device density and operating frequency was low enough. But nowadays due to increased integration and operating frequency of integrated circuits, power consumption has become an important factor. Battery operated portable devices which performing the high performance processing task also consumes lots of power. The various methodologies are used to reduce the power dissipation by optimizing the parameters that are related to power consumption of circuit.

The Static RAM is used as a cache memory in the processor and also has an application in the embedded system. Due to continuous advances in the integrated circuit technology, the density of SRAMs in embedded application has grown substantially in recent years. The SRAM block is becoming indispensable block in the system-on-chips (SoCs). The larger density SRAM block has a highly capacitive bit lines and data lines. The dynamic power of SRAM is mainly due to charging and discharging of highly capacitive lines.

To perform the write operation in the SRAM cell to flip the data value, nearly full voltage swings is required on the bit line. This full voltage swing on the highly capacitive bit lines will consumes a greater amount power according to law of CV2f. Thus voltage swing reduction is an effective way to decrease the power dissipation. The current mode sensing technique is proposed to give the small voltage swing on the bit lines during write operation. In the proposed method the layout and simulation is done for the one bit line pair for three different methodologies. The bit line interference of selected cell with adjacent selected and non selected cell is also checked out. The proposed current conveyor method has shown an improvement in terms power dissipation over the voltage write and current read (VWCR) and current write and current read (CWCR) method without comprising the performance.

Author: Bhatia, Atul (200611024)
Title: Spectral Estimation Using WRLS Algorithms for Multiband Detection; x, 85 p.; 2008.
Supervisor: Chakka, VijayKumar
Call No.: 621.38224 BHA
Acc. No.: T00161
Keywords: Weighted recursive least square; Adaptive notch filter; Recursive prediction error; Spectral

estimation. Multiband estimation; Spectral theory (Mathematics) Regression analysis; Speech processing systems; Adaptive signal processing; Adaptive filters; Algorithms; Adaptive signal processing -- Mathematics.

Abstract: Signal parameter estimation in the presence of noise has been a key area of research. Many applications have benefited from advancements made in this field within the last two decades. The method proposed in the thesis introduces a new family of infinite impulse response adaptive notch filters that forms multiple notches using a second-order factorization of an all-pass transfer function. The filter sections are orthogonal to each other. The resulting notch filter requires few parameters, facilitates the formation of the desired band rejection filter response, and also leads to various useful implementations (Cascaded, Parallel, Using Filter banks). In this thesis a variation of cascade type structure is used. The algorithm proposed for adaptively estimating filter coefficients is based on WRLS method. Fast convergence along with lower bias as compared to previous algorithms is achieved. This property is particularly attractive for detection and tracking of unknown sinusoids. Computer simulations are provided to illustrate the performance of the proposed adaptive notch filters in terms of bias, speed of convergence, and tracking capability. Also simulations for detection of multiband signals is given.

Author: Bhawsar, Vishal (200611002)
Title: Nonuniform Sampling and its Reconstruction Methodologies; xi, 84 p.; 2008.
Supervisor: Chakka, VijayKumar
Call No.: 621.38223 BHA
Acc. No.: T00146
Keywords: Signal theory (Telecommunication) – Mathematics; Sampling; Time-series analysis; Digital signal processing.

Abstract: Alias-free DSP (DASP) is a methodology of processing signals digitally inside bandwidth that are wider than the famous nyquist limit of half of the sampling frequency. This topic has benefited from a strong research revival during the past few years. DASP is facilitated by suitable combination of non-uniform sampling and appropriate processing algorithms. In this thesis different stretegies to perform nonuniform sampling and its spectrum analysis are studied. We examine the problem of reconstructing a signal from non-uniform samples. A polynomial interpolation based reconstuction techniques are presented. Its performance are compared with the other previous papers on reconstruction technique on the basis of MSE criteria and Complexity of algorithm.

Author: Choudhary, Vivek Kumar (200611029)
Title: FPGA Implementation of Direct Sequence Spread Spectrum Techniques; v, 34 p.; 2008.
Supervisor: Dubey, Rahul
Call No.: 621.38456 CHO
Acc. No.: T00179
Keywords: Field programmable gate arrays -- Computer-aided design; Verilog (Computer hardware description language) Neural networks (Computer science) Field programmable gate arrays; Mobile communication systems; Telecommunication systems; Computer networks – Management; Modeling -- Computer programs; Sensor networks; Simulation methods; Wireless communication systems.

Abstract: This work presents the performance, noise analysis and FPGA implementation of Direct Sequence Spread Spectrum technique. Performance of signal increases as increasing parity bits in Hamming code algorithm. Increasing parity noise goes reduce therefore received signal close to its original value, but adding parity band-width requirement also increases. This work is bases on the IS-95 standard for CDMA (Code Division Multiple Access) Digital Cellular.

Author: Desai, Amee Anilbhai (200611049)
Title: Web Services Policy in Grid; x, 71 p.; 2008.
Supervisor: Chaudhary, Sanjay
Call No.: 006.76 DES

Acc. No.: T00178
Keywords: Web services; Computer networks -- Access control; Computer systems -- Access control; Computer security; Grid architectures Grid Computing Internet -- Security measures; Computer networks -- Security measures; Web services -- Security measures; Electronic data processing -- Distributed processing.

Abstract: Service-oriented computing enables service providers to publish their business functionalities in the form of abstract contracts, which can be discovered by service consumers based on open and standard protocols. Enterprise may be running a number of multiple business processes in parallel, which may require different services to fulfil the functionality.

There are number of factors that both service provider and service consumer should consider before they interact with each other. Web services standards are used for acquiring interoperability among services for large scale adoption of architecture. In Web service selection phase without the use of policy, a service consumer selects the Web service which matches the functional requirements. For satisfying non-functional requirements of a service consumer, policy is used in Web service selection phase. This thesis proposes an approach and architecture to select Web services based on WS-Policy in grid. Service selection depends on metadata and policy. There is a need for dynamic selection services based on runtime environment such as content (semantics), and contract (policy). This thesis proposes an approach and architecture for dynamic selection of services based on policy and semantic .To provide better search, query, composition, and management, there is a need for mechanism to group these services based on the requirements of clients and business processes. This thesis proposes context and location based approach for service grouping and group notification. Context and location provide powerful mechanism for the better search, query, grouping and group notification to the services, and it allows customization based on user preferences, role, and location to improve personalization. The thesis proposes context and location driven grid business process to aggregate information from multiple sources according to the preferences of clients. A policy based service grouping approach is used to aggregate services. For achieving location driven approach, this thesis develops virtual organization and for specifying preferences in virtual organization, a policy is used.

Author: Dhaka, Kalpana
Title: Symbol Detection in MIMO Systems; x, 56 p.; 2008.
Supervisor: Chakka, VijayKumar
Call No.: 621.3840285572 DHA
Acc. No.: T00147
Keywords: Space time codes; MIMO systems; Wireless communication systems; Antenna arrays; Modulation (Electronics).

Abstract: Multiple input multiple output symbol detection methods are observed under frequency flat fading AWGN channel condition. The modulation method employed is Quadrature amplitude modulation (QAM). The various symbol detection techniques are compared to observe their behavior under AWGN channel condition condition. Maximum likelihood (ML) symbol detection method gives the best performance but because of its high complexity it can't be used. Sphere decoder reduces the complexity to some extent providing similar performance as ML estimate. The other methods used are Zero forcing and Minimum mean square stimation. These two methods when used successively for interference cancellation improves performance to large extent along with reduction in the cost. The technique employed for successive detectionis devised by bell laboratory hence it is called as V-BLAST method. Maximum a posteriori when used along with V-BLAST MMSE algorithm further improves the performance. These methods even works well under Rayleigh channel condition. Finally, the simulation results for performance of V-BLAST under both the channel condition are observed for all the symbol detection techniques. To increase the diversity for improved performance space time trellis code are employed. Their performance is observed for QPSK modulation scheme.

Author: Doshi, Kaushal J. (200511036)
Title: A Tool to Find Dimension of Capacitors For Switched Capacitor Band Pass Filter; viii, 80 p.; 2008.
Supervisor: Nagchoudhari, Dipankar
Call No.: 621.3815324 DOS

Acc. No.: T00145
Keywords: Switched capacitor circuits; Low voltage integrated circuits; Switched capacitor filters; Metal oxide semiconductors; Integrated circuits.

Abstract: The switched capacitor (SC) circuits find their applications in many fields. Due to their lower size at low frequencies, higher density can be achieved compared to active RC counterparts. Still there are nonlinerarities in SC circuits, many which are due to error in fabrication process. As will be explained later, the performance of SC circuits depends on capacitance ratios instead on absolute values; hence as designer, we are interested in matching the capacitance ratios rather than absolute values.

This tool which we designed takes care that the width and length of the capacitors it gives as output, has area ratios and perimeter ratios equal for all capacitor pairs, thus taking care of the proper matching of all capacitor.

Author: Gupta, Akshay Kumar (200611005)
Title: Low Cost Design of IFFT module for Dolby AC-3 Decoder; vii, 45 p.; 2008.
Supervisor: Dubey, Rahul
Call No.: 621.38932 GUP
Acc. No.: T00149
Keywords: Sound -- Recording and reproducing -- Digital techniques – Standards; Data compression (Computer science) Data compression (Telecommunication) -- Standards.

Abstract: Dolby AC-3 is a flexible audio data compression technology capable of encoding a range of audio channel formats into a low rate bit stream. AC-3 is the de facto audio standard for high-end digital consumer multimedia equipment. In this thesis work we have implemented 8 point FFT module using radix-2 algorithm. This work also shows the implementation of 128 point IFFT module using split radix algorithm.

Author: Gupta, Punam Sen (200611017)
Title: Design of Low Power and High Speed Decoder for 1Mb Memory; vii, 43 p.; 2008.
Supervisor: Nagchoudhari, Dipankar
Call No.: 621.395 GUP
Acc. No.: T00156
Keywords: Electronic circuit design; Coding theory; Decoders (Electronics) Coding; Computer programs; Large scale integration; Linear integrated circuits -- Design and construction; Memory (Computers) Semiconductor devices; Very large scale integration.

Abstract: Technology scaling is accompanied by rise in leakage power dissipation. This thesis proposes a voltage controllable circuit in the feedback path of the decoder, which drastically reduces the standby leakage current with minimum loss in speed and slightly overheads in terms of chip area. This circuit generates slightly lower supply voltage when the load circuitry is in the standby mode thereby raises the Vt of the CMOS transistors and hence reduces leakage power dissipation The overall power dissipation of a 7x128 decoder is reduced from 0.928mW to 0.584mW for 1Mb Memory with voltage controllable circuit, namely 37% lowering in power dissipation. The operating voltage for the design is 1.2 V. Layout is done in magic 7.1 version in 180nm technology. The simulations are done in LT spice.

Author: Jayanthi Ravishankar, V. (200611040)
Title: Frequency Offset Estimation in OFDM Signals Using Particle Filtering Along With Resampling Methods; vii, 34 p.; 2008.
Supervisor: Chakka, VijayKumar
Call No.: 621.38216 JAY
Acc. No.: T00170
Keywords: Digital modulation; Radio frequency modulation -- Receivers and reception; Synchronous data transmision systems; Synchronization; Data transmision systems; Multiplexing; Telecommunications; Functions, Orthogonal; Wireless LANs; Orthogonalization methods; Orthogonal frequency division multiplexing; Mobile communication systems; OFDM.

Abstract: Frequency offset is one of the main effects the Bit Error Rate(BER) in orthogonal frequency division multiplexing (OFDM). There are many applications which depend on OFDM. The present method describes the estimation of frequency offset for OFDM irrespective of the distribution of the channel noise. This method uses Particle Filtering for the estimation of frequency offset. As Particle Filter is a non-linear and non-Gaussian estimator, there will be no constraint on the channel noise. This method also uses the resampling methods, which are essential in modifying the weight approximates during the iterations. Here the performance of the Particle Filter in estimating the frequency offset for the OFDM is observed along with the resampling methods.

Author: Joshi, Ashwini Kumar (200611039)
Title: An Efficient ASIC Implementation of Advanced Encryption Standard; viii, 88 p.; 2008.
Supervisor: Nagchoudhari, Dipankar
Call No.: 005.82 JOS
Acc. No.: T00184
Keywords: Computers -- Access control – Standards; Data encryption (Computer science) – Standards; Computer security – Passwords; Computer security – Standards; Computer algorithms -- Testing.

Abstract: In spite of the many defense techniques, software vulnerabilities like buffer overflow, format string vulnerability and integer vulnerability is still exploited by attackers. These software vulnerabilities arise due to programming mistakes which allows security bugs to be exploited. Buffer overflow occurs when buffer is given more data than the capacity of it. Format string vulnerability arises when data supplied by attacker is passed to formatting functions as format string argument. Integer vulnerability occurs when program evaluates an integer to unexpected value due to integer overflows, underflows, truncation errors or signed conversion errors.

The hardware based solution called tagged architecture protects a system against mentioned vulnerabilities. In tagged architecture, each memory byte is appended with one tag bit to mark data that comes from I/O. Whenever I/O supplied data is used to transfer control of a system or to access memory, an alert is raised and program is terminated. This thesis proposes a weakness of tagged architecture by finding false positives and false negatives on it. It also proposes the improvements to the tagged architecture to avoid found false positives on it. The prototype implementation of improved tagged architecture is done in SimpleScalar simulator. The SimpleScalar simulator is a architectural simulator. The security evaluation is done for tagged architecture and improved tagged architecture through benchmarks and synthetic vulnerable programs.

Author: Kalariya, Vishalkumar Ramshbhai (200611016)
Title: Multi Band Fractal Antenna For Satellite Application; ix, 40 p.; 2008.
Supervisor: Gupta, Sanjeev
Call No.: 621.38254 KAL
Acc. No.: T00155
Keywords: Antenna design; Microstrip antennas; Ultra-wideband antennas; Adaptive control; Wireless communication systems; Satellite communication; Spacecraft antennas; Communication networks.

Abstract: Fractal Antenna is the current topic for the research engineering because Fractal Technology allow us to design miniature antennas and integrate multiple band in single device. This antenna is a type of Micro strip antenna so it can be mount on the same PCB on which other RF components are mounted. There is not exact method to predict the resonance frequency of the Fractal antenna. Current research work tell that the prediction of resonance frequency of the Antenna is made from the simulation result. But in this work we try to predict the resonance frequency by mean of Network connection method. In this method each small segment of fractal shape antenna is treated as the single square patch and by analysis the separate patch and combing the total impedance by mean of Network connection method and the prediction of the resonant frequency is done by this thesis work.

By using the Cavity model approach we find the impedance of the separate patch and by the Network connection model approach we can combine the total resistance and find the input impedance of the fractal antenna and we are trying to design the Multi band Fractal antenna for the L band(1.4GHz), C band(5.35GHz) and last is X band(9.65GHz) which is resonating at three

band of frequency by this method.

Author: Mathur, Rahul (2006110047)
Title: Performance Analysis of TCP over Enhanced UMTS Network; viii, 43 p.; 2008.
Supervisor: Jotwani, Naresh
Call No.: 621.3845 MAT
Acc. No.: T00176
Keywords: Global system for mobile communications; Universal Mobile Telecommunications System; Cryptography; Computer network protocols; Mobile communication systems; Computers -- Access control.

Abstract: The increase in demand and overwhelming response of 3G mobile networks has made it a technology which would drive the future of mobile communication. On the other hand the popularity of the Internet has also increased with type of services it is providing. Internet mainly relies on TCP/IP protocol which is the backbone of almost all NRT packet services.

The designer of TCP made it for wired networks only, so it lacks the capability to handle the wireless nature of the link. The performance decreases when the error in the wireless link occurs in burst. To recover error more reliably wireless link uses some recovery mechanism at the link layer like ARQ. The error recovery by doing retransmission at the link layer may increase the latency and adds to the overall RTT of packet. TCP treats these sudden increase in delays as a congestion indication, and starts it congestion recovering mechanism which indeed not required here. TCP lowers the number of packet to be transmitted by lowering the Congestion Window and hence causing a degraded performance.

Many solutions have been proposed to alleviate the problem. But all have some flaws at their own level. Introduction of HSDPA in 3G UMTS system, has raised up some hopes regarding TCP performance. The technical features that HSDPA has brought proven to be a performance enhancer for TCP. The effect of ARQ delay is minimized by the introduction of a new error mechanism at the physical layer. This error mechanism uses the principles of chase combining and incremental redundancy to increase the probability of successful decoding of the data block. The TTI duration has been changed from 10ms to 2ms so that overall delay reduces to a great extent. More efficient algorithms have been proposed to cope with the time varying channel conditions which can be utilized to schedule users to maintain an optimal use of system resources. The thesis investigates the influence of these features and also the effect they imposes on TCP performance.

Author: Narmawala, Zunnun A. Raoof (200611007)
Title: Network Coding based Multicast in Delay Tolerant Networks; viii, 50 p.; 2008.
Supervisor: Srivastava, Sanjay
Call No.: 004.6 NAR
Acc. No.: T00151
Keywords: Computer networks – Reliability; Computer network protocols.

Abstract: Delay Tolerant Networks (DTN) are sparse ad hoc networks in which no contemporaneous path exists between source and destination most of the time. In DTN, connectivity graph of the network changes over time either due to mobility or sleepwakeup cycles of the nodes. Mobile Ad hoc Network routing protocols such as AODV, DSR etc. fail in such scenario because they try to find end-to-end path before data transmission which is non-existent in DTN. So, routing protocols proposed for DTN follow 'store-carry-forward' paradigm in which two nodes exchange messages with each other only when they come into contact. In the process, 'Single-copy' schemes maintain only one copy of the message in the network at any time while 'Multi-copy' schemes spread more than one copy of the message. While Multi-copy schemes improve chances of delivery, communication overhead and buffer occupancy are quite high for these schemes. We propose Multi-copy routing protocol for multicasting in DTN called "Multicast In Delay TOlerant NEtworks (MIDTONE)" which uses 'Network coding' to reduce this overhead without impacting the performance. Network coding is a mechanism in which nodes encode two or more incoming packets and forward encoded packets instead of forwarding them as it is. We also propose a novel packet purging scheme which takes advantage of features of network coding to increase buffer

efficiency. As simulation results suggest, our protocol achieves significantly less delay to deliver all the packets in infinite buffer case and higher delivery ratio in finite buffer case compared to non-network coding based Multi-copy scheme.

Author: Panchal, Bhavi (200611020)
Title: Design of Voltage Reference Circuits; xi, 42 p.; 2008.
Supervisor: Parikh, Chetan D.
Call No.: 621.39732 PAN
Acc. No.: T00159
Keywords: Metal oxide semiconductors, Complementary; High voltages; Integrated circuits; Electronic circuit design; Low-voltage integrated circuits Bipolar integrated circuits.

Abstract: Shrinking device dimensions in advancing CMOS technologies require lower supply voltages to ensure device reliability. As a result, analog circuit designers are faced with many challenges in finding new ways to build analog circuits that can operate at lower supply voltages while maintaining performance. Bandgap references are subject to these head-room problems especially when the required supply voltage approaches the bandgap voltage of silicon. However, the bandgap reference working with a low supply voltage often has a higher temperature coefficient than that of a traditional bandgap reference. This has resulted in the development of new temperature-compensated techniques.

Piecewise linear curvature correction method is simple yet robust technique which was previously available in bipolar technology. This research work describes a Novel CMOS bandgap reference which uses piecewise-linear curvature compensation scheme for second order correction. In standard 0.18µm CMOS process, the reference, with 1.8 V supply produces an output of about 928 mV, which varies by 160 µV from -25 °C to 150°C. It dissipates 150 µW and has a DC PSRR of -46 dB.

Author: Pandit, Vivek Kumar (200611041)
Title: Design of Multi Standard RF Front End Receiver Using Novel Low IF Topology; xiv, 69 p.; 2008.
Supervisor: Gupta, Sanjeev
Call No.: 621.38412 PAN
Acc. No.: T00171
Keywords: Radio circuits -- Design and construction; Radio -- Receivers and reception; Radio detectors; Radio -- Transmitter-receivers; Wireless communication systems -- Equipment and supplies.

Abstract: This thesis presents the multi-standard receiver architecture and the corresponding RF front-end design supporting Bluetooth and IEEE 802.11a WLAN standards. To maximize the level of component share in the proposed multi-standard receiver, the corresponding standards is analyzed and applied to the proposed multi-standard receiver architecture. Low-IF architecture is chosen for both Bluetooth and IEEE 802.11a WLAN, respectively. The system specifications and the building block specifications is derived from the corresponding standards and verified by spreadsheet models taking into account of major design issues such as image-rejection, intercept points, noise figure and gain. The simulation results prove the validity of the system analysis and the proposed multi-standard receiver architecture.

Author: Ramesh, R. (200611011)
Title: Design Of Low Voltage High Performance Voltage Controlled Oscillator; ix, 48 p.; 2008.
Supervisor: Nagchoudhari, Dipankar and Mandal, Sushantha Kumar (Visiting Faculty)
Call No.: 621.38412 RAM
Acc. No.: T00153
Keywords: Oscillators, Electric; Electronic circuit design; Radio frequency oscillators -- Design and construction; Low-voltage integrated circuits; Amplifiers (Electronics) Phase-locked loops; Metal oxide semiconductors, Complementary; Electronic circuits – Noise; Radio circuits; Electronic circuits.

Abstract: In this thesis an ultra low voltage differential capacitive feedback VCO is being proposed .The VCO operates at very low supply voltage of 0.6V.The VCO uses techniques like Forward Body Bias

(FBB), and capacitive feedback to achieve high performance in terms of phase noise and output voltage swing. It uses differential MOS varactors for frequency tuning due to which all low frequency noise such as flicker noise gets rejected. Inductor was designed and it was simulated in IE3D electromagnetic simulator to achieve good Quality factor. This VCO achieves a very low phase noise of -119dBc/Hz@1-MHz offset frequency, power consumption of 3.27mW, and tuning range of 6% .All the circuit simulations of VCO were simulated in SpectreRF using TSMC 0.18µm CMOS technology.

Author: Ranjith, P. (200611021)
Title: Designing of an efficient power clock generation circuit for complementary pass transistor adiabatic logic carry save multiplier; x, 56 p.; 2008.
Supervisor: Nagchoudhari, Dipankar, and Mandal, Sushantha Kumar (Visiting Faculty)
Call No.: 621.39732 RAN
Acc. No.: T00160
Keywords: Integrated circuits -- Very large scale integration -- Design and construction; Low voltage integrated circuits -- Design and construction; Logic circuits -- Design and construction; Bipolar integrated circuits; Metal oxide semiconductors, Complementary.

Abstract: This thesis presents a novel four-phase power clock generator for low power adiabatic logic without using inductors. The power clock generator is designed using current mirror arrangement of PMOS and NMOS transistors. Different logic families have been studied and Complementary Pass-transistor Adiabatic Logic (CPAL) is chosen to implement an adiabatic carry save multiplier as it gives less energy dissipation per cycle than other logic families at higher load capacitances and higher loads. The power clock is designed for CPAL which requires four phase trapezoidal waveform. An 8-bit carry save multiplier is designed which is used as load to clock generation circuit. The clock generator consumes equal energy per cycle at all frequencies. The control logic required for clock generation circuit is also simple to implement. Conversion efficiency of the order of 10% is obtained for an equivalent load capacitance of 2pF. The simulations are done using LT spice in 0.25µm TSMC technology. Layouts are drawn in MAGIC 7.1.

Author: Rao, Parth A. (200611050)
Title: Energy Efficient data gathering Protocol for Wireless Sensor Network; v, 50 p.; 2008.
Supervisor: Srivastava, Sanjay
Call No.: 621.384 RAO
Acc. No.: T00186
Keywords: Sensor networks; Wireless communication systems; Wireless LANs; EIGRP (Computer network protocol) Routers (Computer networks) Wireless communication systems -- Quality control.

Abstract: Wireless Sensor Network is made up of hundreds and thousands of miniature electronic devices called node, which have sensors built on them. Functionality of a sensor is entirely application dependent. They can perform a large number of functions from measuring the forces of nature like temperature, humidity, geophysical activity, sound vibrations to motion detection and military surveillance. Apart from sensing or measuring, the nodes are responsible for efficiently collecting the sensed data by performing appropriate activities on the collected data and there by weeding out redundant data so as to reduce transmission overload on nodes. Thus the nodes are responsible for gathering data and routing the data to the base station.

Data Gathering can be performed in number of ways after nodes are deployed in the sensing field depending on their application. The manner in which nodes are deployed in the sensing field also affects the lifetime of the sensor network. It is not always possible that all nodes after deployment in the sensing field are able to communicate with the base station. Moreover efficient utilization of the energy is a must for sensor nodes, because these sensors are battery powered devices, and after they are deployed in the sensing field it is not feasible to change the battery of the nodes. So energy preservation of nodes in sensor network is a crucial requirement to be taken care of. The other prime matter worth considering is that during the whole life time of the sensor network care should be taken that load distribution on all the nodes in the sensing field is equal. All nodes should either die randomly at random location in the sensing field at random time intervals, or all nodes should start dying at more or less the same time.

We have proposed an energy efficient protocol for data gathering in wireless sensor networks, which through hierarchical cluster formation reduce the number of high energy transmissions per round of data gathering and takes care of the load balancing issue by randomized rotation of the cluster heads. Routing of data is done in multi-hop fashion to ensure that the most remotely located node is also able to communicate with the base station through the best available intermediary nodes.

Author: Rathore, Akhil (200611042)
Title: Design of High Speed I/O Buffer; ix, 33 p.; 2008.
Supervisor: Parikh, Chetan D.
Call No.: 621.381528 RAT
Acc. No.: T00172
Keywords: Memory management (Computer science) Bipolar transistors – Design; Metal oxide semiconductors – Design; Digital electronics – Design; Random access memory; Electronic circuit design; Electric current converters; Computer architecture.

Abstract: In high speed serial transmission of data, output buffer creates the bottleneck. Current Mode Logic (CML) buffers have gained wide acceptance in most high speed serial interfaces as they reach speed of the order of Gbp/s. CML buffers achieves high speed due to low output voltage swing which reduces transition time.

Presently CML buffers are designed with differential architecture and uses different bandwidth extension technique (inductive peaking, negative miller capacitance, active feedback) to increase the speed. At high frequency, input output coupling limits the bandwidth due to miller effect because of gate to drain capacitance.

The proposed design incorporates the architecture which reduces miller effect, hence achieves high bandwidth. In this topology a source follower drives a common-gate stage which is an example of 'unilateral' amplifier, that is, one in which signal can flow only in one way over large bandwidths. It reduces unintended and undesired feedback.

This CML buffer is designed for OC-192/STM-64 application to be used in limiting amplifier which is a critical block in optical system. OC-192/STM-64 works around 10Gbps.

Author: Ravikanth, Sivangi (200611030)
Title: Orthogonal Frequency Division Multiplexing Synchronization Techniques; vii, 55 p.; 2008.
Supervisor: Chakka, VijayKumar
Call No.: 621.38216 RAV
Acc. No.: T00166
Keywords: Digital modulation; Radio frequency modulation -- Receivers and reception; Synchronous data transmision systems; Synchronization; Data transmision systems; Multiplexing; Telecommunications; Functions, Orthogonal; Wireless LANs; Orthogonalization methods; Orthogonal frequency division multiplexing; Mobile communication systems.

Abstract: Synchronization plays a major role in the design of a digital communication system. Essentially, this function aims at retrieving some reference parameters from the received signal that are necessary for reliable data detection. The OFDM is very sensitive to symbol timing and frequency offset. The loss of orthogonality among the subcarriers causes degradation of the OFDM system performance. so, the timing and frequency offset must be estimated and compensated before demodulating the OFDM signals. This report presents the study of different synchronization schemes for OFDM receiver. Different methods like Schmidl-Cox synchronizer, The Coulson synchronizer, The Minn-Zeng Bhargava synchronizer, Blind carrier offset estimation using unused subcarriers etc. Matlab experiments are conducted to study the performance of different synchronization schemes. The simulations results shows that Blind estimation method is more advantage over training symbol and Cyclic Prefix (CP) based methods in terms of Bandwidth saving.

Author: Rawat, Nitin (200611025)
Title: FPGA Implementation of Image Compression Algorithm Using Wavelet Transform; xi, 60 p.; 2008.
Supervisor: Dubey, Rahul
Call No.: 621.3670151 RAW
Acc. No.: T00162
Keywords: Image compression; Image processing; Wavelets (Mathematics) Image processing – Mathematics; Image compression – Mathematics; Image transmission; Data compression (Computer science).

Abstract: This work presents FPGA implementation of image compression algorithm by using wavelet transform. Here the emphasis has been made on algorithmic encoding, the first step of image compression problem. The transform that has been used for algorithmic encoding is the „Discrete Wavelet transform□. The Wavelet family which has been used for this purpose is the „Haar Wavelet family□. Various issues involved in hardware implementation of Wavelet Transform such as fractional interpretation, signed Q-format, range of gray scale values, memory requirement and addressing schemes have been discussed. A functional unit has been proposed which calculates the Wavelet transform of input pixel values. An efficient use of „Block RAM□ present in FPGA has been proposed by placing the initial pixel values and then placing the computed Wavelet transform values back in this memory itself. A suitable way to tackle the issue of storing intermediate wavelet transform values by using a buffer memory has been suggested. This removes the need of having an external memory and thus the time required in accessing this memory reduces drastically. A special emphasis in order to use this memory in accordance with the requirement of image processing algorithms has been made by deriving the necessary addressing schemes. This is done in order to have the correct placement of transformed values in memory. Here we have used the Dual port feature of the Block RAM with one port providing multiple pixel values to the functional unit and other being used to write transformed values one at a time. Along with this, the DCM available in FPGA has been used to address issue of skew and „set up time□ involved with the clocks in digital design. A delayed version of system clock is sent to memory so that all addresses and enable signals calculated with reference to system clock are stable when active edge of clock is received by memory. All these modules are incorporated in a top module which provides the Wavelet transform of an image. The modelling of the architecture has been done by using Verilog Hardware Description Language and the functional simulation has been done by using Xilinx ISE Simulator. The synthesis of the design has been done by using Xilinx Synthesis Tool (XST) of Xilinx. The total amount of the resources being utilized is reported and it comes out well within reach of Spartan 3E FPGA, our target device. The maximum clock frequency which can be used for the design comes out to be 23 MHz which is quite high for a compute intensive algorithm like Discrete Wavelet Transform.

Author: Reddy, Pandu Ranga M. (200611046)
Title: Video Compression using Color transfer based on Motion Estimation; xi, 62 p.; 2008.
Supervisor: Mitra, Suman K.
Call No.: 621.388 RED
Acc. No.: T00175
Keywords: Digital video; Video compression; Data compression (Telecommunication) Image processing -- Digital techniques; Wavelets (Mathematics) Transformations (Mathematics) MPEG (Video coding standard) Video compression – Standards; Digital video – Standards; Coding theory.

Abstract: Many compression techniques were developed in last decade and are being used in many applications like HDTV, Videoconferencing, Videophone, multimedia work stations and mobile image communications. It is also certain that digital video will have a significant economic impact on the computer, telecommunications, and imaging industries. Compression that is obtained by standard compression schemes for color video can be further increased if we can take the advantage of color information of successive images of a scene. The color of the objects in the present frame will be almost similar to the color of it in previous frame. So color can be applied at decoder, even if the information is not known for all frames of a scene. The main objective of this thesis is to propose schemes for different profiles of MPEG-2 which uses color transfer techniques. The proposed schemes are tested with different sequences and are compared with the MPEG-2 coded sequences.

Author: Sattaru, Annamnaidu (200611045)

Title: Single Frame Super Resolution; vi, 49 p.; 2008.
Supervisor: Joshi, M. V.
Call No.: 621.367 SAT
Acc. No.: T00185
Keywords: Image processing; Image processing -- Data processing; Imaging systems -- Image quality; Image processing -- Digital techniques; Resolution (Optics).

Abstract: Super-resolving an image from single frame observation image. In many cases more than one low resolution observations may not be available, need high spatial resolution images e.g. medical imaging, remote sensing etc.. We obtain the estimate of the high frequency (edges) contents by learning the wavelet coefficients from a database of similar or arbitrary high resolution images. We then employ a suitable regularization approach for edge preservation as well as for ensuring spatial continuity among pixels. The learnt wavelet coefficients are used as edge prior. An Markov Random Field (MRF) model is used for spatial dependence. The final cost function consists of data fitting term and two regularization terms, which is minimized by global optimizing (Gradient Decent) method. The experiments conducted on real images show considerable improvement both perceptually and quantitatively when compared to conventional interpolation (Bicubic Interpolation images) methods. The advantage of the proposed technique is that unlike many other super-resolution techniques, a number of low resolution observations are not required. Finally instead of MRF we used Inhomogeneous markov random field(IGMRF) for maintain the spatial dependency effectively in super-resolved image, the results show that its better than MRF prior.

Author: Sejpal, Riddhima (200611019)
Title: Exploring Small World Effect in Ad Hoc Network; viii, 47 p.; 2008.
Supervisor: V. Sunitha
Call No.: 004.6 SEJ
Acc. No.: T00158
Keywords: Computer networks; Sensor networks; Wireless communication systems -- Design and construction.

Abstract: Small world is a highly clustered i.e., a densely and fully connected network, with low degree of separation between the nodes. These networks have inherited the high clustering property of regular networks and low average path length property of random network, thus giving an efficient network compared to both. The parameters used to quantify the above mentioned properties are clustering coefficient C and characteristic path length L respectively.

Small world property was noticed in many real world networks and many people tried to convert the existing networks into small world networks. Similar model is used in this thesis, which adds a single node with a long radio range in n × n square grid network along with other nodes having small and same radio range. Considering this network model, we have worked to come up with mathematical equations of the parameters L,C and efficiency e of network before and after adding the long radio range node in a square grid network.

Author: Sesha Sai, Aduru Venkata Raghava (200611012)
Title: Design of Low Voltage, Low Power, Wide Band CMOS LC VCO using Active Inductors; ix, 48 p.; 2008.
Supervisor: Parikh, Chetan D.
Call No.: 621.38412 SAI
Acc. No.: T00154
Keywords: Oscillators, Electric; Electronic circuit design; Metal oxide semiconductors, Complementary -- Design and construction; Signal processing -- Digital techniques; Integrated circuits -- Very large scale integration -- Design and construction; Radio frequency oscillators -- Design and construction; Low-voltage integrated circuits; Amplifiers (Electronics) Phase-locked loops; Metal oxide semiconductors, Complementary; Electronic circuits – Noise; Radio circuits; Electronic circuits.

Abstract: In this thesis the design of low-voltage, low-power, wide-band CMOS LC VCO using active inductor has been proposed. The oscillator is based upon the classic LC-tuned negative-resistance topology, with a novel active inductor using a low-voltage gyrator topology with a feedback

resistance, where feedback resistance is realized by a NMOS operating in triode region whose bias voltage tunes the inductance of the active inductor and hence the frequency of VCO. The simulation results shows that this VCO operates in a 1.19 GHz to 2.49 GHz , while consuming 1.09 mW from a 1.2V power supply. The VCO's phase noise level is -86.9 dBc/Hz at 1 MHz offset from a 1.55 GHz carrier. The deviation of the phase noise is 11.5 dBc/Hz during this tuning range. All the circuit simulations of VCO were simulated in SpectreRF using TSMC 0.18µm CMOS technology.

Author: Shah, Hina Rajiv (200611032)
Title: Object Classification in Image using Information Slicing; viii, 45 p.; 2008.
Supervisor: Banerjee, Asim and Mitra, Suman K.
Call No.: 621.367802856 SHA
Acc. No.: T00168
Keywords: Image processing -- Digital techniques; Visual texture recognition -- Data processing; Algorithms; Optical pattern recognition.

Abstract: Human visual system, in real world, identifies objects by their shapes, sizes and colors. More than often we identify objects around us specifically by using contextual knowledge of the objects. For example, an area of vegetation when seen in satellite imagery, if surrounded by a barren land might be identified as a region of woods, while the one surrounded by urban area would be considered as a park.]

Conventional methods of classification for images, use the spectral information given in by pixels and their neighbors as information for classification, be it supervised or the unsupervised method. However, the information thus used seems to be incomplete in a sense that only local information of the pixels is used for the purpose. Moreover, this does not imitate human visual system of identifying the objects. An attempt has been made here to perform supervised Classification of Objects in Images using Information Slicing. These objects are obtained by using proper segmentation methods. Feature vectors from these segments representing the objects are calculated. Feature vectors are then given as an input to a classifier for classification.

Information slicing for classification involves identifying regions in the feature space for the definite classes. Basically this method consists of partitioning the feature space every time into several regions and identify these regions as to which class the region belongs to. If for a region, it cannot be identified what class it belongs to, the feature space is partitioned again with higher number of regions defined in the feature space. This training leads to a very simple classification procedure. Classification then consists of find-and-assign problem. This feature space partitioning method for classification is a supervised one, and effectively works on highly overlapped data.

Real time systems when described by feature vectors for the purpose of classification, more than often tend to have overlapping regions between the classes. The classifier hence performs misclassifications. This is also true for classes of objects in images. This dissertation deals with study of Object Classification in Images using Information Slicing method for classification. This includes identification of objects in an image, extracting meaningful features and finally classifying the objects on the basis of proper subset of features extracted using feature space partitioning.

Author: Shah, Sapan (200611048)
Title: A Queueing Theoretic Framework for Performance Analysis of Mobile Ad Hoc Networks with Finite Buffer Nodes; ix, 43 p.; 2008.
Supervisor: Lenin, R. B. and Srivastava, Sanjay
Call No.: 004.65 SHA
Acc. No.: T00177
Keywords: Ad hoc networks (Computer networks) -- Security measures; Ad hoc networks (Computer networks) -- Quality control; Wireless LANs. Routing (Computer network management) Ubiquitous computing; Computer network protocols; Computer network architectures; Computer networks -- Quality control; Mobile ad-hoc networks; Dynamic networks; Optimum Link State Routing; Multipoint relays; Quality of Service; Pervasive computing.

Abstract: Wireless Ad Hoc network is a decentralized wireless network which allows nodes to join and create networks without any infrastructure. These kinds of networks are advantageous because they can be readily deployed anywhere, anytime. Mobile Ad Hoc Network (MANET) is a special type of ad

hoc network where nodes are mobile. Due to mobility of the nodes, network topology may change rapidly and unpredictably.

MANETs are expected to plat a vital role in a variety of applications and are therefore studied extensively. It is imperative to analyze these networks, to assess the suitability of their use in different scenarios and to identify the techniques to improve their performance. In last few years, many models have been proposed to analyze MANETs. Many of then have an unrealistic assumption of an infinite buffer in each node. Moreover, in MANETs, as nodes are mobile, a packet may revisit the same node which creates feedback loops of a packet. These loops make modeling and analysis of MANETs difficult as the network becomes cyclic.

This work analyzes MANET with finite buffer nodes. Open finite queuing network with gated queue, intermittent links and servers is used. The expansion method technique has been used to study the open finite queuing network with stable links and servers. We modify the method for intermittency. Numerical results are derived and compared with simulation results to show effectiveness of the method.

Author: Shah, Tejaskumar (200611028)
Title: Improvement of Tagged Architecture for Preventing Software Vulnerabilities; ix, 101 p.; 2008.
Supervisor: Mathuria, Anish
Call No.: 005.8 SHA
Acc. No.: T00165
Keywords: Computer architecture; Computer engineering; Computer security; Computer software – Development; Computer networks -- Security measures; Computer software – Testing; Computer software -- Reliability.

Abstract: In spite of the many defense techniques, software vulnerabilities like buffer overflow, format string vulnerability and integer vulnerability is still exploited by attackers. These software vulnerabilities arise due to programming mistakes which allows security bugs to be exploited. Buffer overflow occurs when buffer is given more data than the capacity of it. Format string vulnerability arises when data supplied by attacker is passed to formatting functions as format string argument. Integer vulnerability occurs when program evaluates an integer to unexpected value due to integer overflows, underflows, truncation errors or signed conversion errors. The hardware based solution called tagged architecture protects a system against mentioned vulnerabilities. In tagged architecture, each memory byte is appended with one tag bit to mark data that comes from I/O. Whenever I/O supplied data is used to transfer control of a system or to access memory, an alert is raised and program is terminated. This thesis proposes a weakness of tagged architecture by finding false positives and false negatives on it. It also proposes the improvements to the tagged architecture to avoid found false positives on it. The prototype implementation of improved tagged architecture is done in SimpleScalar simulator. The SimpleScalar simulator is a architectural simulator. The security evaluation is done for tagged architecture and improved tagged architecture through benchmarks and synthetic vulnerable programs.

Author: Sharma, Abhishek (20061106)
Title: Study of Bayesian Learning of System Characterisitcs; ix, 59 p.; 2008.
Supervisor: Jotwani, Naresh
Call No.: 519.542 SHA
Acc. No.: T00150
Keywords: Bayesian statistical decision theory; Machine learning; Neural networks (Computer science) Artificial intelligence; Bayes theorem; Inference; Probability theory; Statistical analysis.

Abstract: This thesis report basically deals with the scheduling algorithms implemented in our computer systems and about the creation of probabilistic network which predicts the behavior of system. The aim of this thesis is to provide a better and optimized results for any system where scheduling can be done.

The material presented in this report will provide an overview of the field and pave the way to studying subsequent topics which gives the detailed theories on Bayesian networks, learning the Bayesian networks and the concepts related to the process scheduling.

Bayesian network is graphical model for probabilistic relationships among a set of random variables (either discrete or continuous). These models having several advantages over data analysis.

The goal of learning is to find the Bayesian network that best represents the joint probability distribution. One approach is to find the network that maximizes the likelihood of the data or (more conveniently) its logarithm. We describe the methods for learning both the parameters and structure of a Bayesian network, including techniques for learning with complete data also. We relate Bayesian network methods for learning, to learn from data samples generated from the operating system scheduling environment.

The various results produced, tested and verified for scheduling algorithms (FCFS, SJF, RR and PW) by an Operating System Scheduling Simulator implemented in programming language JAVA. Here, the given code is modified according to requirements and fulfilling the necessary task.

Author: Sinha, Ajay Kumar (200611044)
Title: A High Speed 512 point FFT Single Chip Processor Architecture; viii, 54 p.; 2008.
Supervisor: Nagchodhari, Dipankar and Mandal, Sushantha Kumar (Visiting Faculty)
Call No.: 621.382202854165 SIN
Acc. No.: T00174
Keywords: Fourier series; Fourier transformations; Fourier transformations -- Data processing; Microprocessors – Design; Algorithms; Signal processing -- Digital techniques.

Abstract: This thesis present a fully parallel novel fixed point 16-bit word width 512 point FFT processor architecture. The 512 point FFT is realized by decomposing it into three 8 point FFT units. This approach reduces the number of required complex multiplication compared to the conventional radix-2 512 point FFT algorithm. It uses an ROM unit for storing the twiddle factor. The proposed architecture is designed in XILINX 8.2i using Verilog and it is functionally verified with the MATLAB. The floorplanning and timing estimation of each basic module of the proposed architecture is done based on the macro element at 0.25 CMOS technology. The core area of this chip is 99.02 mm2. The processor compute one parallel to parallel (i.e. when all input data are available in parallel and all output data are generated in parallel) 512-point FFT computation in 422 clock pulse in 4.69sec at 90 MHz operation.

Author: Soni, Shraddha (200611031)
Title: Formal Analysis of Two Standardized Protocols Using Strand Spaces; x, 103 p.; 2008.
Supervisor: Mathuria, Anish
Call No.: 005.8 SON
Acc. No.: T00167
Keywords: Data protection; Computer security; Computers -- Access control; BAN logic Protocols.

Abstract: To achieve secure communication it is critical to provide protocols which are secure against attacks. Formal methods are helpful in finding whether or not a protocol is secure. The first formal method for this task, namely BAN logic was proposed by Burrows, Abadi and Needham. However, it is well known to have deficiencies. The most recent deficiency was found by Teepe who showed that the hash inference rule of BAN logic is unsound. This rule was first used in the analysis of CCITT by Burrows, Abadi and Needham. Later it was also used in the analysis of SET by Agray, Hoek and Vink.

This thesis proposes a simple modification to the BAN hash rule to remove its unsoundness. We demonstrate that the modified rule captures the inference that the original rule intended to capture for the above protocols. The deficiency of BAN in proving security guarantees cannot be overcome by just modifying the rules. It would therefore be preferable to have proof of security using alternate methods which are more rigorous than BAN logic. To this end, we provide proofs of correctness of the above protocols using the strand space technique proposed by Fabrega, Herzog and Guttman.

Author: Srivastava, Abhishek (200611035)

Title: Embedding binary trees and caterpillars into the hypercube; vi, 40 p.; 2008.
Supervisor: V. Sunitha
Call No.: 511.52 SRI
Acc. No.: T00182
Keywords: Parallel processing (Electronic computers); Computer algorithms; Parallel algorithms; Graph theory-Hypercube; Surfaces, Algebraic; Algorithms; Computational complexity.

Abstract: Embedding graphs is an important and well-studied theory in parallel computing. Finding the embedding of trees into hypercubes is an important, interesting and difficult problem. This work studies the embedding of binary trees and caterpillars into hypercubes. We give an embedding for a special type of binary tree into its optimal hypercube. We also present embedding of generalized ladders as subgraph into the hypercube. Through an embedding of caterpillars into generalized ladders, we have obtained an embedding of a class of caterpillars into their optimal hypercube.

Author: Srivastava, Amit (200611033)
Title: Application of BTrees in Data Mining; vii, 44 p.; 2008.
Supervisor: Jotwani, Naresh D.
Call No.: 005.74 SRI
Acc. No.: T00180
Keywords: Data mining; Web databases; Database System; Algorithms in Java; Arrays; Binary Trees; Graphs; Trees and External Storage; Queues; Sorting.

Abstract: As massive amount of information are becoming available electronically, techniques for making the decision to analyze statistics on the large dataset are tending to be very complex. Making of such a decision requires more disk accesses in the main memory. So there is a need of such important techniques which can take least number of disk accesses as well as less running time to perform some operations in the main memory.

Building of such a strategic goal oriented decision, there is requisite to classify the information into different classes with the help of some given properties of the information which enabled us to make two BTrees that are running simultaneous. One BTree is used as a classifier for making the decision and another bTree maintains the organization of the information of dataset from where we make the strategic decisions.

Our research embodies around the learning, implementation and usage of advances data structure (i.e. BTree). In our thesis work we have used the binary search approach instead of the linear search takes running time O (T), has enhanced the performance of the BTree during execution of the operations on the BTree.

Author: Srivastava, Anit (200611034)
Title: Collaborative Filtering Approach With Decision Tree Technique; vii, 54 p.; 2008.
Supervisor: Jotwani, Naresh D.
Call No.: 005.74 SRI
Acc. No.: T00181
Keywords: Data mining; Web databases; Database System; Algorithms in Java; Arrays; Binary Trees; Graphs; Trees and External Storage; Queues; Sorting; Filters; Decision making--Computer programs.

Abstract: Rapid advances in data collection and storage technology has enabled organizations (especially e-commerce) to accumulate vast amounts of data. The amount of data kept in computer files and databases is growing at a phenomenal rate because customers are evolving to use e- commerce services. So processing of large number of coustomer's past purchase records is becoming a new challenge in e-commerce. The primary goal of e-commerce services is to build the systems where customers can get their likely recommended products relevant to their past purchase.

We have implemented collaboratives filtering with supervised learning techniques. One of supervised learning techniques is Decision Tree. We have used Decision Tree to cluster similar type of customers according to active customer preferences (or tastes). In our new approach, a collaborative filtering based recommender system will recommended Top-k likely products according to customers preferences (or tastes) by considering past purchase record (or implicit

ratings) of its clustered customers. This system will also recommend or predict Top-k likely products to particular customers by considering the cases when clustered customers have given explicit ratings (or votes) to their previously purchased products.

Author: Uday Kumar, Ch. (200611027)
Title: A 1.5V. 2.4GHz Highly Linear CMOS Down conversion Mixer; x, 50 p.; 2008.
Supervisor: Parikh, Chetan D.
Call No.: 621.38412 KUM
Acc. No.: T00164
Keywords: Integrated circuits; Radio frequency; Metal oxide semiconductors, Complementary -- Design and construction; Low-voltage integrated circuits; Microwave integrated circuits; Microwave integrated circuits -- Design and construction; Very high speed integrated circuits.

Abstract: In the tremendous growth of wireless handheld devices, low power consumption becomes a major consideration in radio frequency integrated circuit (RFIC) designs. This thesis explores low voltage low power RFIC design for CMOS mixer through their applications in a RF front-end transceiver.

A highly linear CMOS down-conversion mixer is designed to operate at 1.5V for single battery solution. Mixer perform frequency down-conversion from a 2.4GHz radio frequency (RF) input signal to a 100MHz intermediate frequency (IF) output signal. The mixer circuit has been simulated in TSMC 0.18µm CMOS technology. Low voltage operation is achieved by using a folded cascode topology. The mixer uses a wide range constant gm cell at input RF stage to increase the linearity (IIP3) performance. The proposed mixer has 0.92dB conversion gain, 17.7dB noise figure, 3.08 1 dB compression point (P-1 dB), 13.8dBm third-order input intercept point (IIP3) and consumes 8.1mW DC power at 1.5V supply voltage. The design ensures that all the transistors remain in saturation, and mixer does perform satisfactorily for +/-50mV variation of the threshold voltage from the nominal value for both NMOS and PMOS transistors. The mixer is simulated for +/- 50mV threshold voltage variations for both NMOS and PMOS transistors. Temperature effects on this circuit were also investigated.

Author: Upadhyay, Ankur (200611038)
Title: Use of Collaborative Filtering for Targeted Advertising; viii, 51 p.; 2008.
Supervisor: Jotwani, Naresh D.
Call No.: 332.01519542 UPA
Acc. No.: T00169
Keywords: Advertising; Finance -- Statistical methods; Bayesian statistical decision theory -- Data processing; Marketing -- Statistical methods; Advertising -- Mathematical models; Information technology.

Abstract: Often in our daily life, we come across situations when we have many options available and are expected to choose one of them. May it be a bookstore, CD shop or a shopping store, even on the internet, the availability of so many genres and a wide variety among every genre poses difficulty in selection of the item. Recommender systems have been providing suggestions but they are not able to provide us options when we are walking through the aisles of a bookstore or a CD shop. Ideally, recommendations should be made available to the customer without giving explicit command.

To provide ease while walking down for shopping in selecting the items based on the item chosen by the customer, the topic focuses on deriving a general model for recommending a product that might save customers money and time along with fulfilling the need. Selection of the product to be advertised by the model is a dynamic decision as it depends on the products kept in the basket. Bayesian approach is used to find the dependencies between items which implements Collaborative filtering and provides real time recommendations on the basis of preferences of earlier customers. The model uses Clustering to limit the complexity of the model that will be built and to aggregate similar items, by grouping customers those who bought items of similar genre. The assumption made is that the selection of the customer is made known to the model in order to process it, to give recommendations; and the recommendations are made known to customers using suitable advertising mechanism.

Author: Vasavada, Tejas (200611026)

Title: Effect of Channel Asymmetry on Reputation based Cooperation Mechanisms in Mobile Ad-hoc Networks; viii, 52 p.; 2008.
Supervisor: Srivastava, Sanjay
Call No.: 621.38216 VAS
Acc. No.: T00163
Keywords: Peer-to-peer architecture (Computer networks); Computer network architectures; Cryptography; Computer security; Signal processing -- Digital techniques; Radio -- Transmitters and transmission – Fading; Modulators (Electronics) Digital communications;
Mobile communication systems.

Abstract: Enforced cooperation among MANET nodes is an active research issue. In applications, where the users have different goals and there is no central authority to control them, users may become selfish. These nodes may not forward packets sent by others and thus affect the basic functionality of the network.

One proposed class of protocols to handle such scenarios is based on reputation functions. In reputation based schemes, nodes maintain reputation values of other nodes. Reputation value of a node is high for nodes that forward the received packets and low otherwise. Nodes with very low reputation values are identified as selfish nodes and isolated from network operations.

In such schemes, every node has to observe whether its neighbour is forwarding packets or not. A node after sending a packet to its neighbour to forward further, increases reputation of neighbour if it overhears the same packet from the neighbour. If it does not overhear the packet, reputation of neighbour is reduced. This is the basic method to observe whether neighbour node is cooperative or not. Here basic assumption is that the channel between two neighbour nodes is always symmetric. This assumption does not hold true due to two reasons: (1) Nodes are moving. Neighbour node may have forwarded the packet but by the time it forwards, either observing node or neighbour or both might move out of each others range. (2) Even if both are in each others range, due to multipath fading, observing node may not overhear the packets forwarded by neighbour node. Thus sometimes even honest nodes may be considered selfish and isolated due to this asymmetry. This reduces throughput of honest nodes.

In this thesis work we have examined the probability of channel asymmetry as a function of ratio r(of inter node distance and transmission range), for given values of relative average velocity of nodes V and Ricean parameter K. Ricean parameter K represents type of the environment i.e. obstructed or unobstructed. We have proposed an enhancement of existing reputation protocol OCEAN. In the enhanced protocol, observing node probabilistically updates reputation of neighbour when it does not overhear. This probabilistic update takes into account probability of channel asymmetry. We have tried to minimize false positives, i.e. honest nodes being detected as selfish. We have shown through simulations that false negatives, i.e. selfish

nodes being detected as honest, do not increase much. We have also shown that how false positives and false negatives change as degree of dishonesty of selfish nodes change. At last, we have shown that throughput levels of honest nodes in original OCEAN protocol and modified OCEAN protocol are almost same.

Author: Verma, Vivek (200611018)
Title: Design of a CMOS Variable Gain Amplifier; x, 103 p.; 2008.
Supervisor: Parikh, Chetan D.
Call No.: 621.395 VER
Acc. No.: T00157
Keywords: Metal oxide semiconductors, Complementary -- Design and construction; Electronic circuit design; Metal oxide semiconductors, Complementary; Digital electronics; Integrated circuits -- Very large scale integration; Metal oxide semiconductor field-effect transistors; Amplifiers (Electronics) Low-voltage integrated circuits.

Abstract: In advanced CMOS technologies as device dimensions are decreasing, requirement for lower supply voltages are increasing to make certain device reliability. So, challenges for analog circuit designers are to discover new techniques to design analog circuits that can operate at lower supply voltages with desired performances. Another challenge for designer is to design a circuit with less power consumption while maintaining desired performance. In this thesis, a CMOS variable gain amplifier is designed to target above challenges.

A fully differential, CMOS variable gain amplifier (VGA) has been designed for a 1.2- volt, low-power, 57-dB dynamic range, and high bandwidth. The VGA comprises of a control circuit, variable gain stages with common-mode feedback circuit. The gain of the VGA varies dB-linearly from -32 to 25 dB with respect to the control voltage, VC. Proposed VGA uses common-mode feedback (CMFB) circuit to fix and stabilize the output DC levels at a particular voltage depending on the input common-mode range (ICMR) requirement and output swing of the VGA. The proposed VGA uses capacitive neutralization technique to achieve high bandwidth operation. This VGA draws 1.25 mA current from a 1.2 V supply. The 3-dB bandwidth varies from 110 MHZ (at 25 dB gain) to 3828 MHz (at -32 dB gain). The proposed VGA is simulated for 0.18μm CMOS technology in LT-Spice with BSIM3V3 model.

2007-2009

Author: Agarwal, Gopal (200711032)
Title: Low Drop-Out (LDO) Voltage Regulator without Off-Chip Capacitor; ix, 34 p.; 2009.
Supervisor: Parikh, Chetan D.
Call No.: 621.381 5 AGA
Acc. No.: T00220
Keywords: Linear integrated circuits -- Design and construction; Electric current regulators -- Design and construction; Low voltage integrated circuits -- Design and construction; Dissertations, Academic -- India.

Abstract: Designing of Low Drop-Out Voltage Regulators (LDOs) operating without a large off-chip capacitor, having a very good transient response and maintaining the loop stability for full load current range in low supply voltage and low quiescent current environment is a challenging task.

The present thesis work proposes a technique to achieve faster loop response during load transients while consuming very less quiescent current. The idea revolves around fast charging and discharging of the large equivalent capacitor at the gate of the pass transistor in response to fast load current transients. The extra circuitry added does not affect the working of main feedback loop in steady state conditions.

The idea is inspired from the Nagraj's idea of achieving high slew rate in operational amplifier which uses an auxiliary circuit to produce large currents in one of the two switching transistors, one for charging and other for discharging the slew rate limiting capacitor in the circuit.

A common source amplifier (having i/p v/s o/p characteristic which closely resembles a digital inverter) followed by the large, normally off switching transistor is used here to overcome the slew rate limitation at the gate of pass transistor.

Author: Anand, Guneshwar (200592014)
Title: Lifetime analysis of wireless sensor nodes using queuing models; v, 35 p.; 2010.
Supervisor: Srivastava, Sanjay
Call No.: 681.2 ANA
Acc. No.: T00239
Keywords: Energy conversion; Wireless sensor networks -- Power supply; Sensor networks; Wireless LANs; Microprocessors -- Energy consumption; Energy transfer; Direct energy conversion.

Abstract:

Prolonging the lifetime of wireless sensor networks (WSN) is one of the key issues for wireless sensor network applications. For increasing the lifetime of network, each node should conserve its energy. Sensor nodes consume different power in different operating modes. It also consumes significant amount of power while switching from one mode to another mode. So it is important that how frequently a node is changing its mode. To address this question we have used queuing theory based control policy, which finds the optimal parameter for switching between modes. We have analysed two different control policies namely, N-policy and T-policy and their effect on the lifetime of a sensor node. In N-policy, a sensor node switches its mode only when total number of packets are N. We find an optimal value of N that minimizes the energy consumption per unit time. Similarly, in T-policy whenever system becomes empty it goes on vaccation for a fixed duration T. It changes its mode only again after T unit of time and stays in the same mode as long as there is a packet. In this case also we find the optimal value of T that minimizes the energy consumption per unit time.

But this improvement in lifetime comes at the cost of longer delay and larger waiting time. We have given the expression for the latency delay. Depending on the application requirement one can tune the parameters to get the best result between the energy saving and latency delay.

Author: Anand Kumar (200711001)

Title: On Size Balanced Binary Search Trees; vi, 35 p.; 2009.

Supervisor: Amin, Ashok T.

Call No.: 005.73 ANA

Acc. No.: T00196

Keywords: Data structures (Computer science); Computer algorithms; Binary systems (Mathematics); Independent data structures; Dissertations, Academic -- India.

Abstract: History independent data structures are useful when security and privacy are of primary concern. Even if an adversary gets copy of the data structure, he cannot obtain any additional information beyond its content. Important property of history independent data structure is that it has no trace visible in its memory layout about the history of operations performed on it. Buchbinder and Petrank [7] in their paper provided lower bounds for obtaining the Strong History Independence for large class of data structures. They also proposed complementary upper bounds for comparison based models and gave an implementation of Weakly History Independent Heap Abstract data structure.

In the paper "A Short Note on Perfectly Balance Binary Tree" by A. P. Korah and M. R. Kaimal [14] an algorithm for insertion of a node in a perfectly balanced binary search tree is presented in which successive data displacement is performed in an inorder fashion to keep the binary tree size balanced. This algorithm has worst case performance linear with the number of nodes in the tree.

Binary search tree is a very useful data structure and is used in many applications such as dictionary, priority queue and supports many operations, such as SEARCH, MINIMUM, MAXIMUM, PREDECESSOR, SUCCESSOR, INSERT, and DELETE. Balanced binary trees such as height balanced binary trees, weight balanced binary trees, etc. support these operations in O (lg n) time in worst-case. Size balanced binary search tree is a balanced binary tree in which number of nodes in one subtree cannot exceed by one than the number of nodes in the other sub tree at every node in the tree. In this thesis, Characterizing Size Balanced Binary Search Tree (SB-BST), I determine the number of Size Balanced Binary Search Trees of a given size. I also provide algorithms to insert into and to delete a node from an SB-BST. Delete operation is followed by Maintain in order to maintain the size balance of Binary Search Tree. These operations require O (n) worst-case run time.

Author: Bhadani, Abhay Kumar (200711033)

Title: Issues of Computational Resource Allocation and Load Balancing in Cloud Computing using Virtualization; x, 68 p.; 2009.

Supervisor: Chaudhary, Sanjay

Call No.: 006.78 BHA

Acc. No.: T00221

Keywords: Cloud computing; VMware vSphere; Virtual computer systems; Operating systems (Computers); Internet; Web services; Grid Computing; Xen (Electronic resource); Load Balancing Technology; Dissertations, Academic -- Masters -- India.

Abstract: With the advent of world wide web, the life of every person has changed drastically. No one can imagine a computer without being connected to the Internet. This dependency is likely to grow in coming years with the adoption of technologies like virtualization and cloud computing. Cloud Computing and Virtualizations one of the foremost technology which has attracted many researchers recently, which is directly going to benefit the end-users and data center service providers. It has many underlying benefits, one of them is directly related to the costs of deploying new servers. Few others are related to harnessing the power of the existing infrastructure and resources. When we look things from server side resource usage, things become quite challenging. Just to meet peak loads, high capacity servers are deployed, which remains underutilized most of the times on an average.

With the help of virtualization technique, we can run multiple instances of different operating systems simultaneously. There are many virtualization tools available, which can be used to

achieve maximum resource utilization. Making efficient use of computing resource (especially computational time) has always been a critical and challenging task. Several scheduling algorithms have been in place, proposed and implemented on one or other Operating Systems from time to time. But, since we have limited processors and things work in concurrent fashion, overload situation can occur hampering the overall objective, performance and throughput of the system. Things become even more challenging when it comes to distributed systems and load balancing.

One of the key commercial player in the virtualization is VMWare, whereas Xen is an open-source free software. There are also few tools like Virtual Box, Linux VServer, OpenVZ, Virtuozzo and few others. Among these the most popular virtual machine monitor is Xen. The likely choice of experimenting with Xen is due to Open Source and wide acceptance by Linux community, and their continuous effort to improve, also it meets the need of industry standards at large.

Consider a hypothetical scenario, where multiple instances of operating systems are running and is being used by the clients over the web in the form of cloud service. The user will use the system as if the whole server and/or system is dedicated to him. The user is completely unaware about the actual physical location of the server on which he is running his applications and disk storage space.

Since, multiple OS are running on a single physical server, and multiple servers are running in the data centre. All connected via high speed network links. At some instance of time, one server may become overloaded, while other server may remain underutilized. This again poses challenge to distribute the load and make things work perfect in this situation. This situation can be handled using load balancing mechanism over the virtual machines. This thesis work tries to find a mechanism to balance the load based on computational time parameter of the virtual machines.

Author: Borana, Lokesh (200711005)
Title: Routing Game In Wireless Network; viii; 32 p.; 2009.
Supervisor: Mitra, Suman K.
Call No.: 004.65 BOR
Acc. No.: T00199
Keywords: Routers (Computer networks); Routing (Computer network management); Computer networks -- Design and construction; Computational complexity; Wireless communication systems; Sensor networks; Game theory; Telecommunication -- Traffic -- Management; Selfish routing; Dissertations, Academic -- India.

Abstract: In this report we have investigated a price based reliable routing game in a wireless network of selfish users. As the nodes are selfish so the path chosen is not the equilibrium path. The main aim is to form a reliable path between a given pair of source and destination. So we have considered reliability and link cost of each node to find the most reliable and shortest path. We have studied an algorithm [1] based on link cost, reliability and selfish behaviour of the intermediate nodes. The pricing mechanism involved in this game is pull based routing game, which is destination driven and source mediated. This means destination node pay to source node and source node pay to all the intermediate nodes. This algorithm is used to find equilibrium path. We simulated the original algorithm and compared the results. We proposed an algorithm to increase the gain by giving reward proportional to link cost and find the shortest path in term of no. of nodes between source and destination.

Author: Chaturvedi, Manish Shivshankar (200711034)
Title: Cooperation Enforcement Mechanisms in Wireless Adhoc Networks; vii, 92 p.; 2009.
Supervisor: Srivastava , Sanjay
Call No.: 621.384 CHA
Acc. No.: T00222
Keywords: Wireless ad-hoc networks; Routing (Computer network management); Computer network architectures; Computer networks -- Quality control; Wireless communication systems; Ad hoc

networks (Computer networks) -- Access control; Routers (Computer networks); Computer network protocols; Dissertations, Academic -- Masters -- India.

Abstract: Wireless adhoc networks are autonomous, infrastrutureless networks where there are no dedicated routers or base stations and nodes are expected to cooperate in Wireless performing routing duties to keep network connected. Cooperation can be assumed if all nodes belong to single authority (e.g. military service or disaster management). But in applications where nodes do not belong to single authority and have limited resources (energy of battery driven devices), like pervasive computing or ubiquitous computing environment, one can not deny possibility of node selfishness. Also as there is no central authority to control node behavior, one can not deny possibility of node maliciousness.

Many cooperation enforcement schemes are proposed in literature, and every scheme is shown to perform better under its own set of assumptions. These assumptions are different for different schemes. So, we aim at defining common set of assumptions and comparing selected schemes on this common ground with respect to packet delivery ratio, energy consumption, routing and other control overhead. We find that with the traffic scenario where nodes do not need services of one another at the same time, the cooperation schemes are not effective in dealing with node selfish ness. We also find that, while dealing with malicious nodes, all cooperation schemes perform better than Dynamic Source Routing(DSR) protocol in improving packet de- livery ratio(PDR), but this improvement comes at the cost of significant increase in routing control packets overhead and energy consumption of cooperation enforcement schemes is higher than that of DSR. Also they fail in punishing misbehaving nodes and the PDR of malicious nodes is comparable to that of good nodes.

Author: Dhairya, Bapodra B. (200711011)
Title: 10-bit high speed high SFDR current steering DAC; ix, 38 p.; 2009.
Supervisor: Parikh, Chetan D.
Call No.: 621.39814 DHA
Acc. No.: T00204
Keywords: Analog-to-digital converters; Digital-to-analog converters; Digital-to-analog converters -- Design and construction; Electronic circuit design; Oscillators; Dissertations, Academic -- India.

Abstract: The Thesis presents an attempt to design a 10-bit High Speed High SFDR Current Steering DAC with a simple and different approach. Most of earlier approaches contain complex design and bulky unary portion. Here an approach tried that uses sub-segmentation of unary part. By using sub-segmentation of unary part, reduction in complex decoder block can be introduced. The issue of synchronization is tackle by a latch that is previously proposed for tackling very high frequency. Here by segmentation of unary part area as well as complexity is reduced for decoder. And the sentence that is always true "Simpler Designs are faster". And reduction in complexity leads to reduction in error sources.

Author: Doshi, Nishant (200711038)
Title: Path Complexity of the Class Binary Search Tree; xii, 31p. ; 2009.
Supervisor: Amin, Ashok T.
Call No.: 005.73 DOS
Acc. No.: T00226
Keywords: Computational complexity; Algorithms; Computer algorithms; Data structures (Computer science); Paths and cycles (Graph theory); Dissertations, Academic -- Masters -- India.

Abstract: Path complexity of a program is defined as the number of program execution paths as a function of input size n. This notion of program complexity has been extended to complexity of a class as follows. Class had data members and data operations. The notion of state for the class is defined based on structural representation of a class. We are assuming only those data operations that change state of a class. The path complexity of a class is defined to be the number of valid input sequences, each of them containing n data operations.

We have analyzed the path complexity of the class Binary Search Tree (BST) based on the algorithms for insert and delete data operations. Later we modify program for delete operation to facilitate determination of path complexity for the class BST. The bounds for the path complexity of the class BST are determined. A program is developed to obtain path complexity of the class BST.

Author: Garg, Neha (200711021)
Title: Identifying Small World Network Properties In Ad-hoc Networks; xi, 83 p.; 2009.
Supervisor: Sunitha, V.
Call No.: 321.384 GAR
Acc. No.: T00210
Keywords: Mobile ad-hoc networks; Computer network architectures; Wireless communication systems; Ad hoc networks (Computer networks) -- Access control; Mobile communication systems; Data transmission systems; Dissertations, Academic -- Masters -- India.

Abstract: Small World Network is a densely connected network with low degree of separation. These types of networks have high clustering property like regular network as well as have low average path length like random network. Thus, Small World Networks are both Locally and Globally ecient as compared to other networks. The above prop- erties can be described using parameters like characteristic path length (L), clustering coefficient (C), local efficiency (Eloc) and global efficiency (Eglob).

Through experiments, done in the past, it has been found that many real world networks exihibit the properties of small world network. This has given rise To finding models for real world networks so that the models reflect small world ness of the real world network. This thesis uses the model of converting a square grid into a small world model by introducing some special nodes. The equations to compute the small world parameters for this model with one and or two special nodes derived in this thesis.

Author: Gupta, Amit Kumar (200611037)
Title: Design Issues in Direct Conversion Receiver; vii, 39 p.; 2009.
Supervisor: Gupta, Sanjeev
Call No.: 621.3841 8 GUP
Acc. No.: T00195
Keywords: Wireless communication systems -- Equipment and supplies -- Design and construction; Mobile communication systems -- Equipment and supplies -- Design and construction; Radio -- Receivers and reception; Radio -- Design and construction; Wireless communication systems; Electric current converters; Metal oxide semiconductors, Complementary; Dissertations, Academic -- India.

Abstract: The wireless system is being rapidly proliferated in our life. The growing of capacity in wireless communication requires a new type of wireless communication method which does not affect current work on circuits and systems that can operate on gigahertz wide signals will undoubtedly be the wave of the future as pressures to supply multimedia services over wireless continue to build. To achieve the goal of single receiver which can act on various different standards the Direct Conversion Receiver (DCR) is the most suitable architecture. The DCR has been known for quite long years. There are number of design issues related to the implementation of DCR. This thesis presents the issues which are related to design of Direct Conversion along with the design issues related to LNA design.

Author: Jain, Akansha (200711010)
Title: Pulse Shaping Design for PAPR Reduction in OFDM; xii, 73p. ; 2009.
Supervisor: Chakka, Vijaykumar
Call No.: 621.382 15 JAI

Acc. No.: T00203

Keywords: Orthogonal frequency division multiplexing; Wireless communication systems -- Design. 3. Wavelength division multiplexing; Orthogonalization methods; Mobile communication systems; Fourier transformations; Computer simulation; Dissertations, Academic -- Masters -- India.

Abstract: Future mobile communications systems reaching for ever increasing data rates require higher bandwidths than those typical used in todays cellular systems. By going to higher bandwidth the (for low bandwidth) at fading radio channel becomes frequency selective and time dispersive. Due to its inherent robustness against time dispersion Orthogonal Frequency Division Multiplex (OFDM) is an attractive candidate for such future mobile communication systems. OFDM partitions he available bandwidth into many subchannels with much lower bandwidth. Such a narrowband subchannel experiences now almost at fading channel. However, one potential drawback with OFDM modulation is the high Peak to Average power Ratio (PAPR) of the transmitted signal: The signal transmitted by the OFDM system is the superposition of all signals transmitted in the narrowband subchannels. The transmit signal has then due to the central limit theorem a Gaussian distribution leading to high peak values compared to the average power. system design not taking this into account will have a high clip rate. Each signal sample that is beyond the saturation limit of the power amplier suersither clipping to this limit value or other non- linear distortion, both creating additional bit errors in the receiver. One possibility to avoid clipping is to design he system for very high signal peaks. However, this approach leads to very high power consumption (since the power amplifier must have high supply rails) and also complex power amplifiers. The preferred solution is therefore to apply digital signal processing that reduces such high peak values in the transmitted signal thus voiding clipping. These methods are commonly referred to as PAPR reduction. APR reduction methods can be categorized into transparent methods here the receiver is not aware of the reduction scheme applied by the transmitter and on-transparent methods where the receiver needs to know the PAPR algorithm applied by the transmitter. This master thesis would focus on transparent PAPR reduction algorithms. The pulse shaping mechanism is used to reduce PAPR. he ct is analyzed in terms of BER.

Author: Jain, Mahavir R. (200711031)

Title: Built-In Self Test Architecture For Mixed Signal Systems; xii, 50 p.; 2009.

Supervisor: Mandal, Sushanta Kumar and Nagchoudhuri, Dipankar

Call No.: 621.381 548 JAI

Acc. No.: T00219

Keywords: Automatic test equipment; Integrated circuits – Verification; Integrated circuits -- Design and construction; Signal processing -- Digital techniques; Mixed signal circuits – Testing; Mixed signal circuits -- Design and construction; Metal oxide semiconductors, Complementary -- Design and construction; Integrated circuits -- Very large scale integration -- Design and construction; Electronic circuit design; Signal generators -- Design and construction; Dissertations, Academic -- India.

Abstract: Built-in self test architecture or BIST as we call them, are the necessity of time since the shrinking sizes of component on-chip with advance in IC technology are making it BIST artistries are being rapidly developed and used for digital circuitry due to well defied fault models and advanced designs tools and techniques available. But with more analog circuitry being built on same platform with digital circuitry, the necessity for BIST architecture of mixed signal system on chip is increasing.

The proposed BIST scheme is developed to test the data converters, both DAC and ADC on chip as well as other analog IP modules depending on specification of design without/least affecting the architecture of actual design and without making use of any complex DSP circuitry. The concept of internet node access based testing of digital blocks is also used for dynamic parameter of DAC like offset voltage and gain error, monotonicity and linearity non-specific BIST scheme. Letter the digital control logic protion of SAR ADC is tested with scan-chain insertion and thus overall functionality of SRA ADC is verified. A simple comparison based method is also proposed for other type ADCs.

For other anlog IPs, we propose IP-based testing where digital to analog converted test signals can be applied depending on specifications of IP design from vendor without affecting architecture

of the design. The output from IPs are taken at different nodes and applied directly to ADC on chip. The digitized output response is then compared with expected response to test the functionality of the DUT and find out its deviation from desired value to achieve pre-defined level of accuracy. The design failing any of the sequence of afore-mentioned test is discarded faulty. The circuitry is designed and evaluated at schematic level using TSMC complementary metal oxide-semiconductor (CMOS) 0.5um technology.

Author: Jain, Priyank (200711008)
Title: Accurate on-chip current sensing technique for Buck Converter; xii, 61 p.; 2009.
Supervisor: Parikh, Chetan D.
Call No.: 621.385 322 JAI
Acc. No.: T00201
Keywords: Pulse circuits; Voltage converters (DC to DC) 3. DC-to-DC converters; Field effect transistors; Dissertations; Academic – India.

Abstract: Current mode bucks converters have many advantages over voltage mode control such automatic over-current protection, Better stability, better line regulation and faster dynamic response. Many different current sensing techniques have been developed and implemented sense the inductor current and use it a feedback loop to regulate the output voltage. Current sensing circuit needs to be highly accurate so as to have good line and load regulation minimum output voltage ripple. The proposed current sensing technique uses a cur mirror (Mp1 and Ma) to mirror the current of the transistor (Mp1) to Ma (with a w ratio of 10000:1, so that carried by Ma, and hence its power dissipation. Is small). Sensed current is converted to voltage using a resistor. Which is used in the feedback loo1 control the width of the pulses? The accuracy of the proposed circuit is98% which gives regulation of 0.8386% and load regulation of 0.3115%. The output voltage ripple of the cur is 10mV.

Author: Lad, Umeshkumar Mangubhai (200711029)
Title: Transaction Based Verification of DA-FIR Filter using AMBA AHB Transactor; x, 39 p.; 2009.
Supervisor: Dubey, Rahul
Call No.: 621.381 548 LAD
Acc. No.: T00218
Keywords: Integrated circuits – Verification; Integrated circuits -- Design and construction; Electronic circuit design; Dissertations, Academic -- India.

Abstract: Transaction based verification is used for faster verification purpose. Reusable transactors are designed and designs are verified at transaction level using these transactors. The test bench are written in higher level language and applied to design via Transactor. Hardware emulators accelerate the use of transaction advantages for the verification people. A number of SoCs and components can be verified with this methodology.

The Device under test (DUT) used here is 5th order signed DA-FIR filter and the Transactor designed is AMBA® AHB™ from ARM. The Transactor is designed as Bus functional model in Verilog and state machine model in C++. The C++ based test bench gives the command (input) for verifying design. The Transactor takes care of the signal needed for applying to DUT. The tool used for the verification is Eve's ZeBu. The verification environment and methodology has been described and compared with the present scenario. Complexity and speed performance are the main constraints for the comparison.

Author: Mahesh Kumar (200711004)
Title: 1V Rail to Rail Operational Amplifier Design for Sample & Hold Circuits; x, 52 p.; 2009.
Supervisor: Parikh, Chetan D.
Call No.: 621.381 535 MAH
Acc. No.: T00198

Keywords: Linear integrated circuits; Operational amplifiers; Bipolar transistors; Operational amplifiers -- Design and construction; Metal oxide semiconductors, Complementary -- Design and construction; Low voltage integrated circuits -- Design and construction; Dissertations, Academic -- India.

Abstract: At low voltage, the input common mode voltage of Operational amplifier is limited which restricts its use as a buffer. This works deals with designing a rail to rail amplifier. The Thesis presents a 1V rail to rail operational amplifier that has been used as a unity gain buffer in the sample and hold circuit for 1V 10 bit 1MSPS pipeline ADC in 0.18µm technology. The Operational amplifier is designed using dynamic level shifting technique which uses an additional input CM adapter circuit for fixing the input common mode voltage. Novelty in the input CM adapter circuit and a low value of gm fluctuation (±0.245%) has been achieved. The Operational amplifier is implemented in standard CMOS technology.

An open loop architecture is chosen for the implementation of sample and hold circuit. The transmission gate switch is used in the sample and hold circuit for reducing the effect of channel charge injection and clock feedthrough. Also, the transmission gate switch offers a low resistance as compared to pMOS or nMOS switches. The sample and hold circuit speed up to 1MSPS has been achieved.

Author: Mishra, Devesh (200711022)
Title: Path complexity of Maximum Segment Sum Problem; viii, 30 p.; 2009.
Supervisor: Amin, Ashok T.
Call No.: 005.73 MIS
Acc. No.: T00211
Keywords: Computational complexity; Algorithms; Computer algorithms; Data structures (Computer science; Paths and cycles (Graph theory); Computer software – Development; Computer software -- Development -- Computer programs; Dissertations, Academic -- Masters -- India.

Abstract: Various software complexity metrics have been proposed in literature. A program complexity measure called path complexity is proposed in [1]. Path complexity P(A,n) of an algorithm A is defined to be the number of program execution paths of A over all inputs of size n. It defines a partition of input space of program A into equivalence classes on the basis of different program execution paths. All the inputs belonging to an equivalence class are equivalent to each other in a sense that they follow same execution path. We present path complexity analysis of four different algorithms for one-dimensional maximum segment sum problem which shows that algorithms with different computational complexity may be equivalent to each other in their path complexity. We also present lower bounds on one dimensional as well as two dimensional maximum segment-sum problems. A different perspective and several observations on one dimensional problem are given

Author: Patel, Brijesh (200711028)
Title: Scalable Routing in Mobile Ad Hoc Networks; x, 63 p.; 2009.
Supervisor: Srivastava, Sanjay
Call No.: 621.382 16 PAT
Acc. No.: T00217
Keywords: Telecommunication -- Switching systems; Computer network protocols; Internetworking (Telecommunication); Data transmission systems; Mobile computing; Mobile communication systems; Dissertations, Academic -- India.

Abstract: In Mobile Ad Hoc Networks (MANETs), performing routing is a challenging task in presence of the varying network parameters like node mobility, traffic and network size. It is very important to analyze the scalability characteristics of the routing protocols with respect to these parameters. ZRP is considered to be one of the most scalable routing protocols due to its multiscoping and hybridization features. We propose a general, parameterized model for analyzing control overhead of ZRP. A generic probabilistic model for data traffic is also proposed which can be replaced by different traffic models. Our analytical model is validated by comparisons with simulations performed on different scenarios. In our simulation results we have observed that the optimal

zone radius lies where the proactive and reactive overhead components of ZRP are approximately equal as observed in [19]. We have also observed that optimal zone radius setting is different under different network conditions. Our simulations show that as the mobility increases the optimal zone radius value decreases, and as the traffic increases the value of optimal zone radius increases. Moreover, if a node operates away from the optimal zone radius setting then it has to bear and ditional routing overhead. Our simulations show that this deviation is quite high in case of low mobility (upto 35%) than in high mobility (upto 23%).

Author: Patel, Pankesh (200711024)
Title: Context Aware Semantic Service Discovery; ix; 91 p. ; 2009.
Supervisor: Chaudhary, Sanjay
Call No.: 004.678 PAT
Acc. No.: T00213
Keywords: Semantic Web; Web services; Semantic Service; Unified model of component composition and service discovery; web service discovery latent semantic kernel support based kernel link analysis data mining; Expert systems (Computer science); Data mining; Dissertations, Academic -- Masters -- India.

Abstract: The aim of service discovery is to discover services based on preferences given by service consumers. Current approaches are using keyword based syntactic methods. Traditional service discovery mechanism acts like a black box which processes input and gives output. Results of service discovery are not based on current situations. Real world is event driven and situations keep on changing in a dynamic manner. Situations effect service providers and service requesters. Hence, service discovery results should be situation aware. By introducing situation awareness (dynamic con- text) in service discovery, one can get relevant results. There is a need to maintain

Dynamically changing context of various services. This work proposes service discovery algorithm, which is based on rule engine. Implemented algorithm gives higher recall value and situation aware results while discovering services.

This thesis is divided into two parts. First part is on Problem Analysis. Part I describes basic concepts of service discovery, context and situation awareness and se- mantic web. Part II proposes service discovery approach, which uses part I concepts. Main key points of parts II are event, situation, and context.

Author: Patel, Sujit Kumar (2007110026)
Title: Self–Calibrating Technique for Digital-to-Analog Converter in Successive Approximation Register Analog-to-Digital Converter; ix, 31 p.; 2009.
Supervisor: Parikh, Chetan D.
Call No.: 621.39814 PAT
Acc. No.: T00215
Keywords: Analog-to-digital converters; Digital-to-analog converters -- Design and construction; Electronic circuit design; Capacitors and Inductors; Dissertations, Academic -- Masters -- India.

Abstract: Successive Approximation Register (SAR) analog to digital converter resolution is limited mainly by the capacitor ratio error; comparator offset voltage and capacitor voltage dependence error. A SAR ADC resolution is limited to 10-bit due above errors. Resolution can be increased by using calibration techniques for these errors. From the calibration of capacitor ratio error and comparator offset voltage 16-bit resolution can be achieved. Calibration of capacitor voltage dependence error is necessary for resolution more than 16-bit.

This thesis proposes the self calibration technique for capacitor ratio error in differential SAR analog to digital converter. Using this calibration technique capacitor ratio error is minimized. Linear voltage coefficient of capacitor is canceled by the differential SAR ADC but, comparator has limitation of finite common mode rejection ratio (CMRR). In this work self calibration of capacitor voltage dependence error is also discussed in detail.

Author: Pateriya, Bhavana (200711009)
Title: Design of CDMA Transmitter and Three Finger Rake Receiver; 55 p.; 2009.
Supervisor: Dubey, Rahul
Call No.: 621.384 5 PAT
Acc. No.: T00202
Keywords: Spread spectrum communications; Code division multiple access; Radio -- Transmitters and transmission -- Fading -- Computer simulation; Wireless communication systems -- Testing -- Computer simulation; Dissertations, Academic -- India.

Abstract: As cellular wireless communication becomes a worldwide communication standard, it is important in studying how data communications happens in a cellular system. In this Thesis work CDMA transmitter and receiver have been designed including the communication channel which include effects of multipath fading and noise. Effectiveness of rake receiver have been verified for varying SNR and with varying the number of fingers. Also the functionality of each block is analyzed.

Author: Pathak, Abhishek (200711018)
Title: Analysis and Modeling of Power Distribution Network and Decoupling Network Design strategies for High Speed Digital and Analog VLSI System; xi, 48 p.; 2009.
Supervisor: Mandal, Sushanta; Nagpal, Raj Kumar and Nagchoudhuri, Dipankar
Call No.: 621.395 PAT
Acc. No.: T00208
Keywords: Semiconductor storage devices; Microprocessors; Application specific integrated circuits; Integrated circuits -- Very large scale integration; Digital communications – Measurement; Data transmission systems; Dissertations, Academic -- Masters -- India.

Abstract: Today's high speed digital and analog VLSI systems are operating in GHz frequency range. With high switching rate of the devices, power distribution network (PDN) impedance causes ripples in power supply. If PDN is not designed properly it can cause false switching, or even it can damage the device permanently. In this thesis whole power distribution network (PDN) for VLSI system has been modeled using RLC equivalent circuits which can be run on any simulation program with integrated circuit emphasis (SPICE) based simulator. Frequency dependent RLC model for printed circuit board (PCB) and package interconnects has been generated, and effects of different geometry and material of interconnects on PDN impedance profile have been analyzed. Model is compared with electromagnetic (EM) full wave simulator both for the accuracy and CPU run time and it is found that model shows good accuracy with very less CPU run time as compared to full wave simulator which can take more than a day to simulate whole geometry. To meet the target impedance of PDN, Strategies for choosing decoupling capacitors and their placement over power plane have been analyzed. Key-words: Power Integrity, power delivery network, voltage regulator, simultaneous switching noise.

Author: Pathak, Swapna (200711007)
Title: Design of Multi-band Fractal Antenna for Satellite Navigation Application; 52 p.; 2009.
Supervisor: Gupta, Sanjeev
Call No.: 621.3854 PAT
Acc. No.: T00200
Keywords: Satellite communication; Frequency variation; Antennas—propagation; Antennas--Technologies; Antennas, Propagation and System Design; Antennas (Electronics) -- Design and construction; Artificial satellites in navigation; Dissertations, Academic -- India.

Abstract: Recent efforts by several researchers around the world to combine fractal geometry with electromagnetic theory have led to a plethora of new and innovative antenna designs. This research proposal has been primarily focused in the analysis and design of fractal antenna

elements. Fractals have no characteristic size, and are generally composed of many copies of themselves at different scales. These unique properties of fractals will be exploited in order to develop a new class of antenna-element designs that are multi-band and/or compact in size. These key issues are the major motivations for the research project which involves the analysis and design fractal antennas in L, S and C-bands.

Author: Rao, K. Ramprasad (200711039)
Title: Vehicle Detection and Tracking; viii; 51 p.; 2009.
Supervisor: Joshi, Manjunath V.
Call No.: 621.367 RAO
Acc. No.: T00238
Keywords: Traffic monitoring -- Equipment and supplies; Traffic monitoring -- Automation; Vehicle detectors; Automobile driving -- Automation; Computer vision; Detectors; Intelligent transportation systems; Motor vehicles -- Automatic location systems; Pattern recognition systems.

Abstract: Real time trafficc monitoring is one of the most challenging problems in machine vision. This is one of the most sorted out research topic because of the wide spec-trum of promising applications in many areas such as smart surveillance, military applications, etc. We present a method of extracting moving targets from a real-time video stream. This approach detects and classifies vehicles in image sequences of trafficc scenes recorded by a stationary camera. Our method aims at segregating cars from non-cars and to track them through the video sequence. A classication criteria based on the features is applied to these targets to classify them into categories: cars and non-cars. Each vehicle can be described by its features. The template region is estimated by means of minimum distance approach with respect to centroid of the obtained blob of the target. Extraction of features from each frame ensures eefficiency of the tracking system.

Author: Roy, Subhash Chandra (200711020)
Title: Design of the Analog Front End Circuit for X-Ray Detectors; xii, 70 p.; 2009.
Supervisor: Parikh,Chetan D.
Call No.: 621.3815 ROY
Acc. No.: T00209
Keywords: X ray detectors; Integrated circuits -- Design and construction; X rays.; X-ray optics -- Design and construction; Analog systems. 6. Electronic circuit design; Electric filters -- Design and construction; Radio circuits -- Design and construction; Linear integrated circuits -- Design and construction; Dissertations, Academic -- Masters -- India.

Abstract: The Thesis presents a novel idea to efficiently read out the value corresponding to incident X-Ray, from X-Ray sensor. A system level solution has been proposed which is unique in itself in terms of approach. A simple design of analog front end circuit for 64 channels, consisting of Charge Sensitive Preamplifier (CSP), Pulse Shaping Amplifier (PSA), Peak Detector, subtractor, Mux and ADC has been proposed. In CSP, Transmission Gate (TG) has been used, in parallel with integrating capacitor, where the NMOS is operating in weak inversion, when TG is supposed to be off. It fulfils the requirements like posing very high ac resistance, providing alternative path for DC leakage current signal, discharging integrating capacitor quickly etc. An amplifier cum level shifter has been used to match the output DC level of CSP with input DC level of PSA. PSA has been implemented as a 4th order Bessel-Butterworth low pass filter, which provides good step response, and hence output is obtained with negligible peaking. High pass filter hasn't been used to avoid low frequency signal loss. A subtractor has been proposed after the peak detector, which is taking care of offset voltages and low frequency noise. This system till the output of shaper is providing a resolution of 1.7% against the specification of 3%.

Author: Sa, Sudhir Kumar (200711040)
Title: Executable Specification Design and Simulation of OFDM Based Communication System; ix, 95 p.; 2009.

Supervisor: Dubey, Rahul

Call No.: 621.38215 SAS

Acc. No.: T00227

Keywords: Orthogonal frequency division multiplexing; Wireless communication systems – Design; Wavelength division multiplexing; Orthogonalization methods; SIMULINK; Computer simulation; Dissertations, Academic -- Masters -- India.

Abstract: The communication system using the OFDM principle is today one of the most important application in communication field. This system has various applications from broadband to 3G and digital TV to Radio LANs. This master's thesis project deals with the implementation of certain specification, algorithmic exploration for WVAN (wireless video area network) in Simulink®. The implemented model and its specification is the reference for the hardware designing and verification. The model used in OFDM based QPSK/16-QAM modulated communication system for the WHD WVAN standard at the High Rate Physical (HRP) layer.

This thesis project describes the functionality of the various communication blocks and the method of data transmission through these blocks. The main purpose of this model is to calculate the BER (Bit Error Rate). The final design which supports the different HRP mode for different code rate and different Modulation scheme can take different length of sub-packets which depends on the HRP mode of Transmission. This model also implements the radix-2 FFT algorithm for fixed point FFT processor. Since the FFT processor cannot be used standalone, so in this thesis it is employed in an OFDM Transmitter and Receiver.

The goal of this report is to outline the knowledge gained during the master's thesis project, to describe a design methodology for the OFDM based communication system for high throughput and best error protection. The functionality of each block of the communication system is written in „C" code and the output data of each block of Simulink Model is compared to 'C' code written output for the same input.

Author: Salimath, Arunkumar (200711012)

Title: 6 Bit 800 MHz Time-Interleaved Analog to Digital Converter based on Successive Approximation in 65 nm Standard CMOS Process; vii, 55 p.; 2009.

Supervisor: Nagchoudhuri, Dipankar and Mandal, Sushanta Kumar

Call No.: 621.381 59 SAL

Acc. No.: T00205

Keywords: Analog-to-digital converters -- Computer simulation; Analog-to-digital converters; Metal oxide semiconductors, Complementary; Analog-to-digital converters – Catalogs; Dissertations, Academic -- India.

Abstract: High-speed analog-to-digital converters (ADCs) with resolutions of 6 bits find wide application in instrumentation, wireless systems, optical communication. This dissertation presents a 6 bit, 8 channel Time-Interleaved ADC based on Successive Approximation that performs analog processing only by means of open-loop circuits that are fully differential, thereby achieving a high conversion rate. The work involves the design of a charge redistribution hybrid-DAC, low offset comparator, shift register based phase generator and the SAR Logic. Designed in 65 nm Standard CMOS STMicroelectronics Process, across all the PVT corners, the ADC achieves SNDR of 36 dB and SFDR of 43 dBFS at 800 MHz sampling rate with low input frequencies. When the input frequency is at 300 MHz the SNDR drops to 32.6 dB. The converter draws an average power of 13.5 mW from a 1.2 V supply.

Author: Saxena, Neha (200711002)

Title: Particle Swarm Optimization Based Synthesis of Analog Circuits using Neural Network Performance Macromodels; xi, 46 p.; 2009.

Supervisor: Mandal, Sushanta Kumar

Call No.: 621.3815 SAX

Acc. No.: T00236

Keywords: Swarm intelligence; Particles (Nuclear physics); Mathematical optimization; Neural networks (Computer science); Semiconductors; Linear integrated circuits -- Design and construction; Electronic circuit design; Analog circuit design; Dissertations, Academic -- Masters -- India.

Abstract: This thesis presents an efficient an fast synthesis procedure for an analog circuit. The proposed synthesis procedure used artificial neural network (ANN) models in combination with particle swarm optimizer. ANN has been used to develop macro-models for SPICE simulated data of analog circuit which takes transistor sizes as input and produced circuit specification as output in negligible time. The particle swarm optimizer explore the specfied design space and generates transistor sizes as potential solutions. Several synthesis results are presented which show good accuracy with respect to SPICE simulations. Since the proposed procedure does not require an SPICE simulation in the synthesis loop, it substantially reduces the design time in circuit design optimization.

Author: Shah, Harshil Anilkumar (200711037)

Title: Testbed based Experimental analysis of Transport Protocols over Wireless Ad hoc Networks; ix, 51 p.; 2009.

Supervisor: Srivastava, Sanjay

Call No.: 621.384 SHA

Acc. No.: T00225

Keywords: Mobile ad-hoc networks; Computer network architectures; Computer networks -- Quality control; Wireless communication systems; Ad hoc networks (Computer networks) -- Access control; Computer network protocols; Data transmission systems; Dissertations, Academic -- Masters -- India.

Abstract: Ad hoc networks are networks with no infrastructure and self-organized in nature. ad hoc networks allow nodes to form network when they come into range of each other provided nodes are configured in ad hoc mode. But these types of network are challenges like high bit error rates, route failures due to mobility, high noise, signal fading and low speed etc. to deal with. Due to this, protocols which are widely used in traditional wired networks may not perform well in MANETs. lower layers like MAC and network layer are either completely changed like 802.11 instead of 802.3 at MAC layer and introducing reactive routing protocols instead of only proactive routing at network layer or significant improvement schemes have been proposed for wireless networks in the existing legacy wired network protocols. But transport layer in MANET is mostly similar to wired networks except some improvements like TCP-ELFN and TCP-Feedback and new transport protocols like Ad hoc-TCP (ATCP), Transport Protocol for Ad hoc networks (TPA) and Ad-hoc Transport Pro- tool (ATP).performance degradation of TCP over wireless links is mainly due to wireless characteristics, TCP features like self-clocking, loss based congestion control, coupling of congestion and reliability, slow start. Several studies have been carried out to evaluate performance of TCP over MANETs but most of them are simulation based studies. But as simulation scenarios can not model exactly the unpredictable nature of wireless environment, we have decided to analyze performance of trans- port protocols over experimental test bed which can be more accurate evaluation of protocols in real-life situation. Performance of 2 transport protocols is analyzed.

Author: Shah, Rahul (200711016)

Title: Comparative Study between Exponential Back off and Dynamic Waiting Strategies for Medium Access in Wireless Ad Hoc Networks; 37 p.; 2009.

Supervisor: Srivastava, Sanjay

Call No.: 621.384 SHA

Acc. No.: T00207

Keywords: Wireless ad-hoc networks; Computer network architectures; Computer networks -- Quality control; Computer networks -- Access control; Wireless communication systems; Ad hoc networks

(Computer networks) -- Access control; Mobile communication systems; Computer network protocols; Dissertations, Academic -- Masters -- India.

Abstract: IEEE 802.11 DCF (IEEE 802.11 Distributed Coordination Function) is widely used MAC protocol for wireless channel access. Although it is developed for single hop networks where all nodes are in the same radio range, it can be directly used for wireless multiphop hoc networks. But performance of IEEE 802.11 DCF in wireless ad hoc networks su ers as it has been developed considering single hop networks only. Many amendments has been proposed to enhance its performance in multihop ad hoc networks. One such scheme is DWMAC (Dynamic Waiting Medium Access Control). In this work, performance of IEEE 802.11 DCF and DWMAC are compared for different network scenarios and traffic patterns. It has been observed that the performance of DWMAC can be further improved if we alter the restricted mode operation of the nodes. We have proposed a new modified protocol DWMAC-Modied and have shown by simulations that DWMAC-Modied offers singnificant improvements.

Author: Sharma, Kapil (200711035)

Title: Cache Performance Evaluation in DSR protocol through Cross-layering for Mobile Ad Hoc Networks; viii, 52 p.; 2009.

Supervisor: V. Sunitha

Call No.: 621.384 SHA

Acc. No.: T00223

Keywords: Mobile ad-hoc networks; Computer network architectures; Computer networks -- Quality control; Wireless communication systems; Ad hoc networks (Computer networks) -- Access control; Mobile communication systems; Computer network protocols; Dissertations, Academic -- Masters -- India

Abstract: Wireless mobile ad-hoc networks are being actively studied by many researchers these days. These networks are suitable to be used in various situations because of (i) their infrastructure-less property and (ii) the mobility of the nodes of the network. However, it is these features which give rise to problems in study of such networks. Further, routing is one of the basic issues in any network design. Inclusion of moving capability to the nodes, make the routing problem more complicated. One is always interested in increasing the throughput and reducing overhead while at the same time solving the issues related to routing. DSR is a protocol that is extensively used for routing in such networks. Cache management and route caching play a significant role in using DSR successively to attain the best behavior for these networks. This thesis looks at and suggests some methods for route caching in DSR.

Author: Sheth, Kavan J. (200711027)

Title: Analysis of Address Allocation Protocols for Mobile Ad Hoc Networks; viii, 71 p.; 2009.

Supervisor: Srivastava, Sanjay

Call No.: 621.382 15 SHE

Acc. No.: T00216

Keywords: Telecommunication -- Switching systems; Ad hoc networks (mobile networks); Mobile ad-hoc networks; Computer network protocols; Internetworking (Telecommunication); Data transmission systems; Mobile computing; Mobile communication systems; MANET 10. Dissertations, Academic -- India.

Abstract: In almost all networks, it is necessary to have a unique identifier for each node. This identifier is used to find out route locating a particular node. So an address is must for any node for unicast communication. Addresses can be preconfigured manually or can be assigned dynamically using a server (e.g. DHCP server). Manual configuration of ad hoc network is not possible for large scale networks. And setting up a server is not possible due to lack of infrastructure in Ad Hoc Networks. So it is necessary to have a mechanism by which we can allocate addresses to the nodes dynamically without any prior setup. Lack of infrastructure and mobility of nodes makes address allocation a challenging task in MANET.

We present worst case message complexity analysis of a number of proposed address allocation

protocols, which can be useful for estimating upper bounds for overhead and latency involved in address allocation as well as partitioning and merging. We also show that the worst case analysis is not a useful indicator of real world performance of the protocols. Buddy approach [5] is one of the many proposed approaches for address allocation. We model DPDA (A Distributed Protocol for Dynamic Address assignment in mobile ado networks)[6], a protocol based on buddy approach, to estimate the overhead involved in address allocation. We conduct simulations in NS-2 and compare with analytical results to validate our model. We perform simplified simulations using Python script which also validates the proposed model. We also do a simulation based comparison of MANETconf (MANET configuration) [8] and DPDA[6] in term of overhead and latency in address allocation, which shows that DPDA causes lower communication overhead and latency than Manetconf.

Author: Singh, Smriti (200711015)
Title: Channel Estimation and Tracking of OFDM and MIMO Systems; xi, 66 p.; 2009.
Supervisor: Chakka, Vijaykumar
Call No.: 621.382 16 SIN
Acc. No.: T00206
Keywords: MIMO systems; MIMO (Multiple Input Multiple Output); Wireless LANs; Orthogonal frequency division multiplexing; Digital communications; Wireless communication systems; Dissertations, Academic -- India.

Abstract: In this thesis, To estimate and track the slow Time varying channels in OFDM and MIMO systems. In first part: we have used a two-dimensional recursive least square adaptive channel estimation technique is used. In orthogonal frequency division multiplexing (OFDM) system, time- and frequency-domain two-dimensional minimum mean square error (2D-MMSE) channel estimation is optimum. However, accurate channel statistics, which are often time varying and unavailable in practice, are required to realize it.2DRLS adaptive channel estimation does not require accurate channel statistics, and at the same time can make full use of time and frequencydomain correlations of the frequency response of time-varying wireless channels. With properly chosen parameters, 2D-RLS adaptive channel estimation can converge into the steady state in only several OFDM symbols time. Although the 2D RLS algorithm creates adaptive letters with a fast convergence speed, this algorithm diverges when the inverse correlation matrix of input loses the properties of positive definiteness or Hermitian symmetry. The diverging of the 2D RLS algorithm same as standard RLS limits the application of this algorithm. We proposed a QR decomposition-based 2DRLS (inverse QR-2DRLS) algorithm, which can resolve this instability. Instead of propagating inverse of correlation matrix of the input signal, it propogates square root of inverse correlation matrix of the input signal. Therefore, this algorithm guarantees the property of positive definiteness and is more numerically stable than the standard RLS algorithm. The parallel implementation of the inverse QR-2DRLS algorithm permits a direct computation of the least squares weight coefficients matrix MATLAB simulations demonstrate that performance of QR-2D-RLS adaptive channel estimation is same as of 2D-RLS adaptive channel estimation and is very effective and suitable for a broad range of channel conditions.

In the second part of the thesis: Since, In MIMO systems, accurate channel estimation is necessary to fully exploit the benefits of spatial diversity offered by such systems. And for time-varying channels, these channel estimates should also be updated accordigly to track the variation of channel. we have used One such method of channel estimation using adaptive SVD updates for channel estimation and tracking of slow-time varying channels in MIMO system. The channel estimates are then further used for symbol detection using V-BLAST/ZF detection algorithm which ensures interference reduction and give better BER vs. SNR performance than SVD based MIMO system.

Author: Singh, Vineet P. (200711030)
Title: A New learning based super resolution using contourlet transform; ix; 33 p.; 2009.
Supervisor: Joshi, Manjunath V.
Call No.: 621.367 SIN
Acc. No.: T00237
Keywords: Image processing -- Digital techniques -- Statistical methods; Wavelets (Mathematics);

Multimedia systems; Computer Imaging, Graphics and Computer Vision; Image processing -- Digital techniques -- Mathematical models; Image reconstruction -- Mathematical models.

Abstract: A new learning based super-resolution reconstruction using contourlet transforms is proposed. contourlet transform provides high degree of directionality. It captures geometrical smoothness along multiple directions and learns the edges present in an image normal to the contour. For learning purpose, training set of low resolution (LR) and high resolution (HR) images, all captured using the same camera, are used. Here two and three level contourlet decomposition for LR images (test image and training image dataset) and HR training images respectively. The comparison of contourlet coeffcients of LR test image from the LR training set using minimum absolute difference (MAD) criterion to obtain the best match contourlet coeffcient. The finer details of test image are learned from the high resolution contourlet coefficients of the training data set. The inverse contourlet transform gives super resolved image corresponding to the test image.

Author: Somani, Gaurav (200711003)
Title: Scheduling and Isolation in Virtualization; xi, 56 p.; 2009.
Supervisor: Chaudhary, Sanjay
Call No.: 005.43 SOM
Acc. No.: T00197
Keywords: Virtual computer systems; Virtual LANs; VMware; Client/server computing; Computer organization; Electronic data processing -- Distributed processing.; Parallel processing (Electronic computers); Real-time data processing; User interfaces & operating systems; Dissertations, Academic -- India.

Abstract: Virtual machine (VM) based server implementation is popular for numerous advantages like fault isolation, efficient hardware utilization, security and ease of management. Virtual machine monitor (VMM) like Xen is a popular virtualization software to manage virtual machines by scheduling them to use resources such as CPU, memory and network. Performance isolation is desirable in virtual machine based infrastructures to meet Service Level Objectives (SLO). In performance isolation, no virtual machine should affect performance of other co hosted virtual machine, which shares the same hardware. Virtual machine schedulers are the key operators in allocating resources among virtual machines. This requires special attention towards scheduling as fairness and resource isolation are the key requirements for which any user virtualizes servers. I/O models are the main bottlenecks in sharing resources among virtual machines. To evaluate isolation property, we need to analyze resource sharing and utilization among virtual machines.

The thesis aims to evaluate the performance isolation achieved by Xen in different scheduler configurations. Experiments are performed using different resource intensive applications to get an insight into isolation. These tests include CPU, Network and Disk I/O intensive benchmarks. Considering the equal importance of I/O applications in virtualized environment, tests for interactive applications in conjunction with CPU intensive applications are also performed. Experiment results show that Isolation is critical when we run I/O application in conjunction with CPU intensive applications. But effective parameter and scheduler configuration can lead towards better isolation as well as utilization. Global balancing of load across all the available physical processors in a physical machine is important characteristic of a scheduler. Xen's Credit scheduler aims to achieve global load balancing on multiprocessor systems. Xen's Simple Earliest Deadline First (SEDF) scheduler can not be used in production environment due to unavailability of this important feature of load balancing. Many applications requires scheduler like SEDF in their implementation to fulfill the requirement of interactive applications. This thesis investigates requirements of this feature and discusses algorithmic design and implementation of a developed user space load balancing program. Experiments show a balance among number of physical processors with better utilization of

Author: Sutariya, Mahesh R. (200711025)
Title: Wireless Sensor Network based Automatic Meter Reading (wSNAMR); 97 p.; 2009.
Supervisor: Ranjan, Prabhat
Call No.: 621.3821 SUT

Acc. No.: T00214

Keywords: Automatic data collection systems; Utility meters -- Data processing; Wireless network Automatic meter reading; Wireless LANs; Sensor networks; OSI (Computer network standard); Routing (Computer network management); Wireless Sensor Network (WSN); Network layer; Dissertations, Academic -- Masters -- India.

Abstract: Automatic Meter Reading is technology evolved from 1995[3] or before, for remote collection of utilities measurement data which involve Electricity, Gas and Water etc. In this process of evolution every time new idea was methodology being used for implementation. In this thesis same task of meter reading will be performed wirelessly by using zigbee standard developed for the low power wireless sensor network. Concentration is on electrical energy. Goal of this work is to have a Remote collection of measured energy value as well as to have an on/off control of this energy supply which will indirectly enable wireless monitoring of energy consumption, prepaid billing etc through web based interface provided. So work will involve development of hardware and firmware and web based software to achieve this functionality. Once energy consumption data is available to us, it can be used for purpose of dynamic tariff management, dynamic load management, power quality monitoring, peak power consumption etc.

Author: Tripathi, Jai Narayan (200711023)

Title: Statistical Co-Analysis, Robust Optimization and Diagnosis of USB 2.0 System for Signal and Power Integrity; xi, 62 p.; 2009.

Supervisor: Dubey, Rahul

Call No.: 621.382 TRI

Acc. No.: T00212

Keywords: Signal integrity (Electronics); Power integrity; Signal processing -- Digital techniques; Digital communications – Measurement; Bit error rate; Application specific integrated circuits -- Power supply; Mixed signal circuits; Semiconductors -- Mathematical models; Data transmission systems; Real-time data processing; Digital computer simulation; Dissertations, Academic -- Masters -- India.

Abstract: Signal Integrity (SI) and Power Integrity (PI) are the most critical issues as semiconductor industry is moving towards higher operational speeds. Signal integrity and power integrity are such issues that should be looked at system level rather than looking at active and passive networks separately. System level analysis becomes a necessity when the individual subsystems work according to specifications, and even after that complete system doesn't work well. System level signal integrity and power integrity problems for high speed serial links have been taken into account in this thesis. Serial links are being used more and more rather than parallel links due to lesser skew and lower pin counts. Specifically USB 2.0 IP is used for this thesis work, but the analysis is generic for all serial links. This thesis considers SI and PI as a dual and a common model is used which considers both SI and PI. A statistical co-analysis of SI and PI for high speed serial links is used, which can be used for a cost effective solution too. Statistical methods are used for efficient simulations and to extract maximum information contents in the least simulation combinations. Based on this co-analysis, the system is diagnosed or modified for better SI and PI. In the end, reflection gain concept is also taken in to account for the diagnosis of the system. All in all, USB 2.0 system is diagnosed for better SI and PI. System level robustness analysis of high speed serial links are taken into account with effect of external environment. A strong correlation between measured and simulated results is shown. A generic methodology for SI and PI for high speed serial links is presented with complete analysis of package, board, termination, squidd card, decoupling network etc..

Author: Verma, Sunil Kumar (200711036)

Title: Design and Implementation Of 128-point Fixed Point Streaming FFT Processor for OFDM Based Communication System; xiii, 73 p.; 2009.

Supervisor: Dubey, Rahul

Call No.: 621.382 15 VER

Acc. No.: T00224

Keywords: Orthogonal frequency division multiplexing; Wireless communication systems – Design; Wavelength division multiplexing; Orthogonalization methods; SIMULINK ; Fourier transformations; Computer simulation; Dissertations, Academic -- Masters -- India.

Abstract: Fast Fourier Transform (FFT) processors are today one of the most important blocks in communication systems. They are used in every communication system from broadband to 3G and digital TV to Radio LANs. This master's thesis project deals with the pipelined, radix-2 algorithmic exploration and the hardware solution for the FFT processor with the FFT size of 2N points, the selection of the scaling schemes based on application requirement is discussed. The designed architecture is functionally verified in Simulink® and the Xilinx® ISE simulator. How to encapsulate the C++ coded algorithms or functions into the Simulink. This FFT processor is used in OFDM based BPSK modulated communication system for the WHD WVAN standard at the Low Rate Physical (LRP) lay.

This thesis project presents the design of the 128 point fixed–point F streaming processor. The final architecture used is the SDF (single path with delay feedback) that implements the radix-2 FFT algorithm. Since the FFT processor can't be used standalone, so in this thesis it is employed in an OFDM Transmitter and the performance is measured for SNR over a range of PAPRs.

The goal of this report is to outline the knowledge gained during the master's thesis project, to describe a design methodology for the fixed point pipelined FFT processors, the scaling choices and how to encapsulate the existing C code into the Simulink environment to measure the performance of fixed-point systems.

Author: Agarwal, Navneet (200811013)
Title: Ant colony optimization in routing algorithms of mobile ad hoc networks; 61 p.; 2010.
Supervisor: Srivastava, Sanjay and Sunitha, V.
Call No.: 621.384 AGA
Acc. No.: T00275
Keywords: Mobile ad hoc network; Wireless communication systems -- Quality control; Mathematical optimization; Ants -- Behavior -- Mathematical models; Ant colony optimization; Optimization combinatoire; Queuing network analysis; Routing algorithms; Mobility models; MANET.

Abstract: The study on performance of On-demand Ant Routing Algorithm for Mobile Ad Hoc Network is done. An ant routing algorithm based on swarm intelligence and especially on Ant Colony Optimization (ACO). It describes a noval on demand Ant colony algorithm for MANETs. This algorithm tries to minimize complexity at nodes and this is achived at exoences of optimality of routing path. Inextensive set of simulation experiment, We try to set parameter of ant routing algorithms and compare Proposed algorithm with DAR,a pre existing on demand ant routing algorithms and with AODV, a reference algorithm in MANETs. The comparition base on optimal path length with respect to control overhead.

Author: Akhani, Janki (200811029)
Title: Negotiation for Resource Allocation on Infrastructure as A Service Cloud; 45 p.; 2010.
Supervisor: Divakaran, Srikrishnan
Call No.: 621.36 AKH
Acc. No.: T00263
Keywords: Service-oriented architecture (Computer science); Web services; Cloud computing; Electronic data processing -- Distributed processing; Information technology -- Management; Information resources management; Composite web services; Resource allocation; Scheduling; Adoption of cloud computing; Utility computing.

Abstract: The Cloud is a computing platform that provides dynamic resource pools, virtualization, and high availability. Cloud computing infrastructures can allow enterprises to achieve more efficient use of their IT hardware and software investments. Infrastructure As A Service (IAAS) cloud providers manage a large set of computing resources. These resources can be provided to cloud consumers on demand in the form of virtual machines. Cloud consumers do not need to manage resources and be worried about the performance issues because they are handled by cloud providers.

Open Nebula is an open source cloud toolkit which can be used to setup an IAAS cloud. It has three components: Open Nebula Core, Virtual Machine Scheduler and Cloud Drivers. Haizea is an open-source resource lease manager, and can act as a virtual machine scheduler for Open Nebula or used on its own as a simulator to evaluate the performance of different scheduling strategies. Haizea supports four kinds of resource allocation policies: immediate, best-effort, advance reservation and deadline sensitive.

To reserve resources in advance using Haizea, consumer submits parameters like amount of resources, start time and duration of a reservation as a request. If one or more parameters can not be satisfied, then Haizea will reject the request. This method is very rigid method because it does not allow negotiation of any parameter. Consumer can resubmit new requests by modifying previously submitted request parameters. Consumer will not be aware of the current resource allocation on provider side so, the chances of new requests getting rejected are more. Thus, it will increase communication overhead between cloud provider and consumer as well as it will decrease resource utilization on provider's side. It will also degrade the performance of a provider in managing many incoming requests due to previously rejected ones.

To overcome the above problems, negotiation can be provided. Negotiation process consists of three components which are negotiation protocol, negotiation objectives and agents' decision making algorithm. The proposed algorithm to generate set of counter offers is a part of decision making model at provider side. It provides set of counter offers to consumer when his advance reservation request gets rejected. It provides set of counter offers considering parameters' flexibilities to maximize the chances of their acceptance. The proposed algorithm for User selection policy is a part of decision making model at consumer side. Consumer can get best suitable offer from set of counter offers using the algorithm of user selection policy. Ranking algorithm is a part of algorithm for user selection policy. Using this ranking algorithm, consumers will get suitable offers sorted according to their needs. It will reduce consumers' efforts to go through all the provided counter offers and choose best suitable one. These algorithms are implemented in Haizea. Experiments are performed to demonstrate the effectiveness of algorithms. The results show that the proposed algorithm to generate counter offers maximizes resource utilization and acceptance of requests compared to rigid and exact methods.

Author: Akula, Sandeep (200811004)
Title: Test Methodology for Prediction of Analog Performance Parameters; 51 p.; 2010.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.3815 AKU
Acc. No.: T00244
Keywords: Electronic circuits; Analog electronic systems -- Testing; Mixed signal circuits -- Testing; Analog electronic systems; Operational amplifiers.

Abstract: Analog testing, the name itself signifies the detection of faults in analog circuits. The aim of this thesis is to increase the test effectiveness and work in the performance parameter space. There are many test methodologies which can detect the faults in the circuit under test (CUT), out of which the test methodologies which can determine CUT performance parameters resulting in enhanced test effectiveness are, predictive oscillation based test methodologies. To detect the catastrophic and parametric faults these methodologies are used. These test methodologies are preferred over other methodologies because the input test stimulus generation is not needed, which reduces the complexity if multiple inputs are applied to the circuit. These test techniques are implemented with prediction process using neural networks which will in turn increases the performance of the circuit under test. The thesis follows with the implementation of the techniques and understanding the methods to increase the test effectiveness. The design process is performed in CADENCE simulation tool with 180nm technology.

Author: Chasta, Neeraj Kumar (200811040)
Title: Design of the High Speed, High Accuracy and Low Power Current Comparators; 61 p.; 2010.
Supervisor: Parikh, Chetan
Call No.: 621.395 CHA
Acc. No.: T00272
Keywords: CMOS Comparators; Comparator circuits -- Design and construction; Metal oxide semiconductors, Complementary; Operational amplifiers -- Design and construction; Integrated circuits -- Very large scale integration; Integrated circuits -- Design and construction; Electronic circuit design

Abstract: Comparators are non linear, decision making analog circuits, which find wide spread application in data converters, data transmission and others. Comparison can be done in terms of "Voltage" or "Current".

A current comparator can be referred as trans-impedance amplifiers which compares applied input currents and generate CMOS compatible output voltage. In this work, study and simulations of various current domain comparator circuits have been done; some of these follow basic analog circuit concepts like current mirroring and Voltage current feedback.

This thesis presents a novel idea for analog current comparison with controlled hysteresis. Proposed circuit is based on current mirror and latching techniques. Comparator presented is

designed optimally in 0.18μm CMOS process in LTspice environment. Designing issues have also been discussed for no hysteresis (or very less hysteresis) case, where comparator gives higher accuracy and speed at the cost of increased power consumption.

In addition to this a simple circuit is proposed which satisfies high speed, high accuracy and low power consumption constraints for the mentioned technology parameters. It utilizes amplification properties of Common gate circuit for generating CMOS compatible output voltage by comparison of applied input signal current and reference current.

Author: Chawla, Charu (200811002)
Title: Moment Based Image Segmentation; 60 p.; 2010.
Supervisor: Mitra, Suman K.
Call No.: 621.367 CHA
Acc. No.: T00242
Keywords: Image processing -- Digital techniques; Image processing -- Statistical methods; Image processing -- Mathematical models; Image segmentation; Image analysis; Computer vision; Machine learning; Computers Visual perception

Abstract: Usually, digital image of scene is not same as actual; it may degrade because of environment, camera focus, lightening conditions, etc. Segmentation is the key step before performing other operations like description, recognition, scene understanding, indexing, etc. Image segmentation is the identification of homogeneous regions in the image. This is accomplished by segmenting an image into subsets and later assigning the individual pixels to classes. There are various approaches for segmentation to identify the object and its spatial information. These approaches employ some features of the input image(s). The concept of feature is used to denote a piece of information which is relevant for solving the computational task related to a certain application. The moment is an invariant feature used in the pattern recognition field to recognize the test object from the database. The key point of using moment is to provide a unique identification for each object irrespective of its transformations. The moment is the weighted average intensity of pixels. It is used for object recognition so far. Now the idea is to use moment in object classification field. The propose method is to compute Set of Moments as a feature for each pixel to get information of the image. This information can be used further in its detail analysis or decision making systems by classification techniques. Moment requires an area to compute it. Hence, window based method is used for each pixel in the image. All possible windows have been defined in which current pixel is placed at different positions and moment is computed for each window representation. The moments define a relationship of that pixel with its neighbors. The set of moments computed will be feature vector of that pixel. After obtaining the feature vector of pixels, k-means classification technique is used to classify these vectors in k number of classes. The different types of moments are used to classify the images namely: Statistical, Geometric, Legendre moments. Experiments are performed using moments with different window sizes to analyze their effect on execution time and other features. The comparative study is performed on various moments using different window sizes. The comparison is done using mismatching between moments, window sizes and their computation time. The implementation is also performed on noisy images. The results conclude that the proposed method probably gives better result than pixel based classification. The Statistical moment gives better result as compared to Geometric and Legendry moment. Its computation time is also less because it does not involve polynomial function in computation. The window size also affects the segmentation. The small window size preserves edge information in segmented image. The computation time and noise tolerance of proposed algorithm also increases as window size increases. Hence, the selections of window size have trade between computation time and image quality. All the experiments have been performed on both gray and colour scale images in MATLAB(R).

Author: Dasi, Shivakrishna (200811010)
Title: Oblique Projection Operator; 46 p.; 2010.
Supervisor: Chakka, Vijaykumar
Call No.: 621.3822 SHI

Acc. No.: T00248

Keywords: Signal processing -- Digital techniques; Block Transmission system; Oblique Projector; Signal representation; Signal recovery.

Abstract: This thesis presents the understanding usefulness of Oblique Projector in signal processing like signal recovery, signal representation and reconstruction. This thesis also presents the different recursive oblique projector methods available in the literature along with this usefulness in the application of time varying channel conditions and additive correlated noise environment.

Author: Dhoot, Vivek (200811021)

Title: Radiation Analysis of Microstrip Active (Amplifier) and Passive (Antenna) Structures; 59 p.; 2010.

Supervisor: Gupta, Sanjeev

Call No.: 621.381 DHO

Acc. No.: T00257

Keywords: Strip transmission lines; Radiation -- Measurement; Microwaves, Millimeter-Waves; Microwave devices -- Computer-aided design; Time-domain analysis; Finite differences; Radio -- Transmitters and transmission -- Design and construction; Radio -- Receivers and reception -- Design and construction; Radio circuits -- Design and construction; Microwave circuits -- Design and construction

Abstract: Analysis of radiation from a microstrip amplifier and a newly proposed microstrip antenna is presented. Microstrip amplifier is analyzed replacing the MMIC structure by an equivalent S2P model and remaining portion being constructed with the original dimensions. A printed monopole antenna using multifractal technique is proposed. This antenna has multiband characteristics covering various wireless applications including WLAN 2.4 GHz and 5.8 GHz applications

Author: Dhumal, Neha (200811034)

Title: Bidding Strategies for Dynamic Spectrum Allocation; 49 p.; 2010.

Supervisor: Srivastava, Sanjay

Call No.: 621.384 DHU

Acc. No.: T00267

Keywords: Antennas (Electronics); Antennas (Electronics) -- Design and Construction; Antennas (Electronics) -- Testing; Wireless communication systems; Microwave circuits; Strip transmission lines; Frequency variation.

Abstract: Dynamic Spectrum Allocation is the process of assigning spectrum licenses in terms of the chunks of the spectrum band to the Wireless Service Providers (WSPs). This allocation assignment is being done as per the WSPs' requirement and this in turn would depend on the end users' applications demand [16]. For Dynamic Spectrum Access, economic framework is needed to make the system feasible under economic terms. This process uses some kind of service pricing mechanism that the service provider can use for the acquisition of the spectrum band and requirement of the end users.

In the Dynamic Spectrum Allocation scenario, the problem is to find the appropriate bidding strategies. The approach to this problem is to simulate the different cases with varying parameters. Here, the interaction between the spectrum owner and providers is modeled through auction model which has been studied in this work whereas the interaction between the providers and end users is based on the demand. This thesis presents the bidding strategies and appropriate prediction method that maximize the revenue and the profit of both the providers as well as the end users. The auction method and different bidding strategies adopted, gives the winning criteria for the providers on how many number of units to bid and the prices for these units. Prediction method for the price uses the concept of probability of winning the particular unit. Simulation results show the comparison between prediction and actual values, revenue and profits of the providers. Among the different auction and bidding methods, the Vickrey auction has been used in this work. In the Vickrey auction method, the allocation of the resources is done efficiently as

compared to other methods and does provide dominant bidding strategy.

Author: Dwivedi, Varun Kumar (200811011)
Title: High Speed Sample and Hold Circuit Design; 38 p.; 2010.
Supervisor: Parikh, Chetan
Call No.: 621.395 DWI
Acc. No.: T00249
Keywords: Digital integrated circuits -- Computer-aided design. 2. Integrated circuits -- Very large scale integration -- Computer-aided design. 3. Analog electronic systems. 4. Metal oxide semiconductors, Complementary. 5. Mixed signal circuits -- Design. 6. Electronic circuit design

Abstract: Sampling of the time-varying input signal is the first step in any type of Analog to Digital (A/D) conversion. For Low Power and high-speed A/D converter, a high-performance Sample and Hold (S/H) circuit is needed as its front-end component.

In this thesis, the high speed sample and hold circuit has been designed, requiring low power as a front end block of pipeline analog to digital converter.

In this work, architectures of sample and hold circuit are studied and issues which limit the performance of sample and hold circuits are discussed.

A fully differential S/H circuit using bottom plate sampling is proposed. The circuit has been designed in order to meet the specification. Amplifiers are studied and folded-cascode amplifier is chosen as an optimum architecture for switch capacitor based sample and hold circuit.

The proposed circuit is designed optimally in a 180 nm CMOS process, in the Cadence Spectre environment. The speed and power achieved are 125 MSPS, 6.8mW respectively.

Author: Gandhi, Nikunj (200811013)
Title: High-Performance Low-Voltage Current Mirror Design; 42 p.; 2010.
Supervisor: Parikh, Chetan
Call No.: 621.3815 GAN
Acc. No.: T00251
Keywords: Linear integrated circuits -- Design; Metal oxide semiconductors, Complementary; Voltage mirror; Symmetrically matched transistor structure; Integrated circuit functional blocks; Linear integrated circuits -- Computer-aided design; Metal oxide semiconductors -- Computer-aided design; Metal oxide semiconductor field-effect transistors; Operational amplifiers -- Design

Abstract: Design of high precision analog circuits requires accounting for the mismatch between nominally identical transistors. In this work, errors affecting CMOS current mirrors due to mismatch between identical transistors are discussed, and circuit techniques to overcome these errors are studied. The dynamic current mirror (DCM) is one of the solutions to overcome mismatch problems.

Dynamic current mirrors contain analog and digital components together so that errors due to process variations, temperature and ageing effect can be cancelled. Various circuit techniques such as op-amp based DCM, reduced transconductance based DCM, and cascode based DCM have been used to improve the performance of current mirrors.

This thesis proposes a novel circuit for a low-voltage high-performance dynamic current mirror design.

The thesis investigates the performance of analog switches at low voltages, and suggests an improved bootstrap switch; errors due to clock feed through and charge injection in the switch are analysed. A new low charge injection, voltage-boosted analog switch is recommended in the dynamic current mirror design. A bulk-driven dynamic current mirror circuit is proposed, and found to be an effective solution at low voltage. The proposed circuit is designed optimally in a 0.18μm CMOS process, in the Cadence Spectre environment. A current copying accuracy of ±0.14% is achieved under worst case conditions.

Author: Gupta, Akshya Kumar (200811027)

Title: A Robust and Secure Watermarking Scheme Based on Singular Values Replacement; 52 p.; 2010.

Supervisor: Raval, Mehul S.

Call No.: 005.82 GUP

Acc. No.: T00274

Keywords: Digital Watermarking; Content Protection; Watermarking Techniques; Intellectual property; Image normalization; Watermark resynchronization; Cryptography and Security; Watermark embedding; Watermark detection

Abstract: Digital watermarking is used to carry information by embedding information into the cover data in a perceptually visible or non visible manner. In today's sea of digital information, there are many problems associated like identity of the owner of content or protecting their rights. In case of any dispute, one can prove their identity by decoding the watermark.

Two most important prerequisites for an efficient watermarking scheme are robustness and invisibility. After embedding the watermark, perceptual quality of the digital content should not be degraded and watermark must be recoverable from the watermarked image even if it is altered or processed by one or more image processing attacks such as compression, filtering, geometric distortions, resizing etc.

In my research work, I have proposed a blind watermarking scheme based on the discrete wavelet transformation (DWT) and singular value decomposition (SVD). In this scheme, Singular Values (SV's) were embedded in the HH band of the watermark for perceptual transparency and robustness.

Although the scheme proves to be robust however it is insecure. An authentication mechanism is proposed at the decoder for security enhancement. It is implemented by using a signature based authentication mechanism. Finally the resulting water- marking scheme is secure and robust.

Author: Kansara, Bena (200811031)

Title: Eye Localization in Video: A Hybrid Approach; 53 p.; 2010.

Supervisor: Mitra, Suman K.

Call No.: 006.37 KAN

Acc. No.: T00265

Keywords: Human face recognition (Computer science); Machine Vision; Face -- Imaging -- Data processing; Biometric identification

Abstract: Location of eyes is an important process for operations such as orientation correction, which are necessary pre-processes for face recognition. As eyes are one of the main features of the human face, the success of facial feature analysis and face recognition depends greatly on eye detection. It is advantageous to detect eyes before other facial features because the position of other facial features can be estimated using eye position and golden ratio. Since relative position of eyes and interocular distance are nearly constant for different individuals, eye localization is also useful in face normalization. Hence, eye localization is a very important component for any face recognition system.

Various approaches to eye localization have been proposed and can be classified as feature based approaches, template based approaches and appearance based approaches. Feature based methods explore eye characteristics - such as edge and intensity of iris - to identify some distinctive features around the eyes. In template based methods, a generic model of eye shape is designed; this template is then matched to the face image pixel by pixel to find the eyes. Appearance based methods detect eyes based on their photometric appearance. Template based and appearance based methods can detect eyes accurately but they are not efficient when considering time factor while feature based methods are efficient but do not give accurate results. So, by combining feature based method with template based or appearance based method, we

can get better results. In the proposed algorithm, we have combined feature based eye LEM approach proposed by Mihir Jain, Suman K. Mitra, Naresh D. Jotwani in 2008 and appearance based Bayesian classi_er approach proposed by Everingham M., Zisserman A. in 2006 to achieve eye localization.

The work of localizing eyes in a video is motivated by some of the applications where eye localization can serve very useful purpose such as to find drowsiness of a person driving a car, eye based control of computer systems for people with motor difficulties. To carry out eye localization, after doing some preprocessing which include frame separation from video and to convert it into gray-scale images, the proposed algorithm is applied on each of these frames. For the experimentation, we have taken videos of few people in the normal blink condition as well as in the sleepy condition. All the videos have been taken in the lab environment. To check the accuracy of the proposed algorithm, we have performed various tests, namely, Wilcoxon signed rank test, Mann-Whitney U test, Kolmogorov-Smirnov test, Sensitivity and False alarm rate tests. And the results of these tests show that the proposed algorithm proves to be quite accurate in localizing the eyes in a video. All the experiments have been carried out in MATLAB.

Author: Khakhkhar, Sandip (200811015)

Title: Bidirectional Service Composition; 53 p.; 2010.

Supervisor: Chaudhary, Sanjay

Call No.: 004.65 KHA

Acc. No.: T00252

Keywords: Web service composition; Electronic data processing -- Distributed processing; Computer network architectures; Service-oriented architecture (Computer science); Ontologies; Semantic composition; Formal methods 8. Web services -- Design; Service composition; Semantic Web Services

Abstract: Service is a network addressable software component to perform a specific task. A service consumes given input parameters, performs specific task based on input parameters and returns the result in terms of output parameters. A service request specifies required task in terms of input parameters that can be provided and output parameters that are required. A service discovery mechanism can be used to find services that can be executed to satisfy service request. Service and service request is match by comparing their input/output parameters. A service request may be complex enough that it can not be satisfied by an individual service. It might be possible to execute a chain of services in a particular order to satisfy service request. This chain of services is referred as composition plan and service offered by executing this composition plan is referred as composite service. The aim of service composition algorithm is to generate a composition plan and generate composite service to satisfy service request.

Services involved in composition plan are selected manually while designing composite service in static composition process. This process consumes considerable amount of time and effort. It is also vulnerable to changes in input/output of services. A dynamic composition algorithm is required that can automatically select services involved in composite plan and generate a composite service on-the-fly. Main issue with dynamic composition algorithms is composition time taken by algorithm to generate a composite service. Composition time indicates duration of the time at which the service request was submitted to the algorithm till the algorithm generate a composite service that can satisfy service request. Composition time depends upon the number of services required to explore in order to find services that can take part in composite plan. Dynamic composition algorithms presented in previous work mainly follows either forward chaining approach or backward chaining approach to find a composite service. Performance of algorithms based on forward chaining approach or backward chaining approach suffers for certain cases to generate a composite service where number of services explored increases exponentially as number of iterations increases.

This work proposes a dynamic composition algorithm that gives consistent performance across all the cases. Proposed algorithm approaches from two directions alternatively, one follows forward chaining approach and other follows backward chaining approach. Composition algorithm following only forward chaining approach or backward chaining approach performs all the iterations in one direction only where as proposed algorithm requires only half number of iterations in both

directions. Algorithm uses two types of matching strategy to compare input/output parameters. First one is based on keyword matching and second one based on semantic matching strategy. Performance of proposed algorithm is evaluated by performing relevant experiments and results are compared with algorithms based on only forward chaining approach or backward chaining approach. Proposed algorithm explores less number of services and takes less composition time compared to algorithms based on only forward chaining approach or backward chaining approach.

Author: Khatri, Nilay (200811046)
Title: Depth From Defocus; 53 p.; 2010.
Supervisor: Banerjee, Asim
Call No.: 621.367 BAN
Acc. No.: T00276
Keywords: Three-dimensional imaging -- Industrial applications; Image processing; Computer graphics; Images, Photographic; Depth of field (Photography); Image reconstruction;Image processing -- Digital techniques -- Mathematical models

Abstract: With the recent innovations in 3D technology accurate estimation of depth is very fascinating and challenging problem. In this thesis, a depth estimation algorithm, utilizing Singular Value Decomposition to compute orthogonal operators, has been implemented to test the algorithm on a variety of image database. Due to the difficulty in obtaining the database, an algorithm is implemented, that attempts to generate various synthetic image database of a scene from two defocused images by varying camera parameters. Thus, providing a researcher with more databases to work upon.

Author: Kulkarni, Rucha (200811039)
Title: Robust Surface Coverage Using Deterministic Grid Based Deployment in Wireless Sensor Networks; 57 p.; 2010.
Supervisor: Srivastava, Sanjay
Call No.: 681.2 KUL
Acc. No.: T00271
Keywords: Wireless communication systems; Sensor networks -- Design and construction; Wireless communication systems -- Design and construction; Algorithms; Sensor networks; Wireless LANs

Abstract: The rapid progress in the field of wireless communication ans MEMS technology has made wireless sensor networks (WSN) possible. These networks may have low cost sensors deployed which are capable of sensing any activity in the vicinity, storing the information etcetera to carry out a certain task. An important problem receiving increasing consideration is the sensor coverage problem, that is, how well the sensors observe the physical space? Coverage can be considered as a measure of quality of service (QoS) of a sensor network [17].

Using equilateral triangle grid based deployment of the sensors, it is necessary to place the sensor nodes such that they are not too close so that the overlapping of the covered area is minimum. But, at the same time, not too far away that it leads to some uncovered areas known as the coverage holes. Thus, the sensing capabilities of the sensor nodes must be fully utilized in order to maximize coverage of the FoI.

To find the coverage of the given uneven surface, the concepts in computational geometry, especially the Voronoi diagrams have been extensively used. When the sensor nodes are deployed using an aircraft, the accuracy of the sensor deployment is affected due to various factors like terrain properties, timing errors in deployment mechanism and more. Hence, it is necessary to take into consideration these placement errors while calculating the coverage of the surface.

Existing work on the coverage of the given surface provides mathematical formulation for 2-D surfaces [5]. But, in real world applications, the surfaces are not 2-D in nature. But have many perturbations. This work intends towards deriving mathematical formulas based on Voronoi Diagram concept for such perturbed surfaces which calculates the value, the sensing radius should be set to, so that the entire region is covered. It also derives formulas when horizontal and

vertical errors are introduced individually and when introduced together.

This work also proposes an algorithm for calculating the coverage of the region under consideration when random errors are introduced in the deployment of the sensor nodes. It also provides information about total area covered for different values of the sensing radius of the sensor nodes. This information is required by different applications having different coverage needs.

Author: Mishra, Ashwini Kumar (200811025)
Title: Design of Row Decoder for Redundant Memory Cell (SRAM); 50 p.; 2010.
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.3973 MIS
Acc. No.: T00260
Keywords: Random access memory; Electronic circuit design; Digital integrated circuits -- Design and construction; Semiconductor storage devices -- Design and construction

Abstract: In the modern technology, the error occurring in memory circuits has increased and the yield of manufacturing has reduced. In order to solve these problems, this thesis proposed a redundancy circuit for faulty row in memory array. The proposed circuit increases the yield and reliability with some loss in speed and overhead in terms of chip area. The circuit designed can test the design whenever a command to test is issued and it will detect and store the faults. Control Circuit designed, checks whether the given address of the memory operation is correct or not. If the address is faulty it replaces the faulty address with the spare address available in the chip.

The existing control mechanism to replace faulty cell in a row replaces the cell bit by bit. But the design here instead of replacing the bit wise cells replaces the entire row containing the faulty cell. This architecture is more useful when there are more faulty cells in a single row.

The row decoder is optimally implemented to reduce the time to access the data from memory.

The operating voltage for the design is 3V. Layout, Simulation of testing circuit and redundant circuit with row decoder has been designed in CADENCE tool for .18µm technology. This Row decoder is working with 2.5GHz frequency.

Author: Nadimenti, Rakesh Kumar (200811022)
Title: Auto Tuning Circuit for Continuous Time Filters; 36 p.; 2010.
Supervisor: Sen, Subhajit
Call No.: 621.367 SHR
Acc. No.: T00258
Keywords: Integrated circuits -- Design and construction; Semiconductors -- Design and construction; Electronic circuit design; Electric filters, Active; CMOS.

Abstract: This thesis presents the design of auto tuning circuit for continuous time filters and is designed for applications that require high linearity and moderate precision. This scheme is used to improve tuning range of 50% and obtain an accuracy of 2-7 %. We use discrete capacitor bank to tune RC time constant instead of varying the g m (Tran conductance) to preserve linearity. The auto tuning circuit consists of analog integrator, voltage comparator, capacitor bank, clock generator and a digital tuning engine. By using tuning logic we can generate a control word and set ON chip integrator capacitor to obtain desired RC time constant. The discrete capacitor tuning scheme is designed in 180nm technology to study about the performance of tuning circuit and is simulated in Cadence design environment.

Author: Nahar, Pinky (200811026)
Title: Column Decoder for Memory Redundant Cell Array; 45 p.; 2010.
Supervisor: Nagchoudhuri, Dipankar

Call No.: 621.38152 NAH

Acc. No.: T00261

Keywords: Electronic circuit design; Integrated circuits -- Fault tolerance; Integrated circuits -- Design and construction; Metal oxide semiconductors, Complementary -- Design; Random access memory; Simulation; Redundancy techniques

Abstract: As the semiconductor technology advances, the yield of memory chip is reducing. The cause of yield degradation is errors in manufacturing process associated with tight geometries. The thesis work proposes a redundancy circuit to enhance the reliability for the faulty columns in memory array. The online testing circuit generates the signals for faulty columns, which enables the redundant circuit to replace faulty with spare column of cells. The redundant decoder and multiplexer provide the path to replace the faulty columns with the spare columns. The novel feature of proposed work is that, input of redundant column decoders depends upon the number of bits for a word output instead of the address signals. The proposed circuit provides the reliability with some loss in speed and overhead in terms of chip area. The operating voltage for the design is 3V. The layout and simulations are performed in CADENCE tool for .1µm technology. The performance parameters of various decoders are performed in LT Spice for .18µm technology.

Author: Nahar, Sonam (200811012)

Title: Disparity Estimation by Stereo Using Particle Swarm Optimization and Graph Cuts; 53 p.; 2010.

Supervisor: Joshi, Manjunath V.

Call No.: 006.37 NAH

Acc. No.: T00250

Keywords: Image processing -- Digital techniques; Computer algorithms; Three-dimensional imaging; Computer vision; Stereo Image Pair Compression; Color image compression; Color re-indexing; Particle swarm optimization; Depth perception

Abstract: Stereo vision is based on the process of obtaining the disparity from a left and a right view of a scene. By obtaining the disparity, we find the distance (depth) of each object point from the camera so that we can construct a 3-D form of a scene. A disparity map indicates the depth of the scene at various points. In this thesis we first discuss the local window based approaches like correlation window and adaptive window for finding the disparity map. These local approaches perform well in highly textured regions, non repetitive and in irregular patterns. However they produce noisy disparities in texture less region and fail to account for occluded areas. We then discuss the particle swarm optimization and graph cuts as global optimization techniques as the tools to obtain better estimates for the disparity map. These algorithms make smoothness assumption explicitly and solve the problem by minimizing the specified energy function. Particle swarm optimization, a bio inspired optimization technique is simple to implement but has high time complexity whereas graph cuts converges very fast yielding better estimates.

In this thesis, we use rectified stereo pairs. This reduces the correspondence search to 1-D. To demonstrate the effectiveness of the algorithms, the experimental results from the stereo pairs including the ones with ground truth values for quantitative comparison is presented. Our results show that the disparity estimated using the graph cuts minimization performs better than the particle swarm optimization and local window based approaches in terms of quantitative measures with fast convergence.

Author: Nathani, Amit (200811036)

Title: Resource Allocation on Infrastructure As A Service Cloud Using Policies; 60 p.; 2010.

Supervisor: Divakaran, Srikrishnan

Call No.: 004.36 NAT

Acc. No.: T00269

Keywords: Service-oriented architecture (Computer science); Web services; Cloud computing; Electronic data processing -- Distributed processing; Information technology -- Management; Information resources management; Composite web services; Resource allocation; Scheduling; Adoption of

cloud computing; Utility computing

Abstract: Conventionally, a cloud refers to an Infrastructure as a service cloud. Infrastructure as a service cloud providers manage a large set of computing resources. These resources can be provided to cloud users on demand in the form of virtual machines. Cloud consumers do not need to manage resources and be worried about the performance issues because they are handled by cloud providers.

Resource allocation in the context of infrastructure as a service cloud means allocating virtual resources namely computing capacity, storage etc. to competing requests based on pre-defined resource allocation policies. In real world most of the Infrastructure as a service clouds rely on simple resource allocation policies like immediate and best effort. Immediate means the resources are allocated if they are available or the request is rejected and best effort means the requested resources are allocated if they are available or the request is placed in first come first serve queue. Sometimes it is not possible for a cloud provider to satisfy all the requests which come to them immediately because of lack of resources. In this case cloud providers can benefit from more complex resource allocation policies.

Haizea is a resource lease manager that tries to address above issues. It uses resource leases as resource allocation abstraction and implements these leases as virtual machines. Currently, it supports four kinds of resource allocation policies: immediate, best-effort, advance reservation and deadline sensitive. The aim of thesis is to extend the current scheduling algorithm of Haizea to support deadline leases in an efficient manner. A dynamic planning based scheduling algorithm is proposed which will admit new leases and prepare the schedule whenever a new lease can be accommodated. The proposed algorithm is implemented in Haizea. Experiments are performed to demonstrate the effectiveness of it. The results show that it maximizes resource utilization and acceptance of leases compared to the existing algorithm of Haizea.

Author: Nema, Swati (200811003)
Title: State Space Based Channel Modelling; 71 p.; 2010.
Supervisor: Chakka, Vijaykumar
Call No.: 621.382 NEM
Acc. No.: T00243
Keywords: Wireless communication systems; MIMO systems; Computer simulation; MOESP; SISO; Space-time model

Abstract: An efficient channel estimation of single-input single output (SISO)/multiple-input multiple-output (MIMO) wireless channel is required for analysis, prediction, fault detection, channel equalization and optimization. This thesis presents a modified recursive MIMO Output-Error State Space Model Identification (MOESP) technique by using fast Givens transformations for LQ update and Lanczos algorithm with modified partial orthogonalization for singular value decomposition (SVD) update. It is based on one of the Subspace System Identification (SSI) technique known as MOESP method. Fast Givens transformation requires 4m multiplications which are less as compared to Givens rotations, as it requires 6m multiplications where m is size of the input vector. Lanczos algorithm with modified partial orthogonalization is applied thereby minimizing the number of vectors to be reorthogonalized for finding the basis for Krylov subspace in the SVD update. Complexity involved in modified partial orthogonalization is O(k:p)3. In existing recursive technique, more number of vectors needs to be orthogonalized by selective orthogonalization method according to the simulation results. Hence, proposed technique offers less complexity and is used for model identification of slow SISO/MIMO wireless channels.

Author: Panarwala, Riyazahmed A. (200811018)
Title: Broadband Spectrum Estimation using Cascaded Integrator Comb Filter; 47 p.; 2010.
Supervisor: Chakka, Vijaykumar
Call No.: 621.382 PAN
Acc. No.: T00254
Keywords: Wireless communication systems; Broadband communication systems; Spread spectrum

communications; FIR filters; Frequency estimation; Signal classification; Spectral analysis; Notch filters; MATLAB.

Abstract: Spectrum estimation using different type of lters is a broad area of research nowadays. In this work, Cascaded Integrator Comb (CIC) lter based narrowband spectrum estimation and CIC band pass lter is presented. Then the broadband spectrum estimation is presented using CIC lters as well as Modied CIC lters with and without white noise. In eigen based methods, eigendecomposition of the autocorrelation matrix is to be obtained. This is a very complex and time consuming procedure while in CIC lter based methods only two additions are required, which signicantly reduces the complexity of the algorithm regardless of the factor M. Complexity based comparison is presented between CIC lter, Modied CIC filter based narrowband estimation and eigenbased frequency estimation methods. All the programs are written in MATLAB.

S

Author: Pandya, Sweta A. (200811030)

Title: Object Segmentation in Still Camera Videos; 25 p.; 2010.

Supervisor: Mitra, Suman K.

Call No.: 621.367 PAN

Acc. No.: T00264

Keywords: Multimedia systems; Digital video; Image processing -- Digital techniques

Abstract: The goal of object segmentation is to simplify and change the representation of an image into more meaningful so that it can easily analyse. Segmentation is the process of partitioning the digital image into multiple segments (set of pixels). It is the foremost step before performing other operations like recognition, scene understanding, tracking, etc. Main purpose of video segmentation is to extract the objects of interest from a series of consecutive video frames. For example surveillance video requires high-level image understanding and scene interpretation for tracking the special events. Another example is of segmenting flower from an image and video in which there are variety of flowers, the variability within a particular flower, and the variability of the imaging conditions – lighting, pose, etc. There are various approaches for segmenting the object from an image. Some of them are histogram based approach, region based approach and graph partitioning approach.

In graph partitioning approach, the image being segmented is modelled as a weighted, undirected graph. Each pixel is represented as a node in the graph, and an edge is formed between every pair of pixels. The weight of an edge is a measure of the similarity between the pixels. Some popular algorithms of graph partitioning category are random walker, minimum mean cut, minimum spanning tree-based algorithm and normalized cut.

In graph partitioning approach, the normalized cut algorithm is used to solve the grouping problem. In this algorithm, image is partitioned into disjoint sets by removing the edges connecting the segments. The partition can be done by finding the splitting point. The optimal solution of the splitting point is computed by solving the Eigen value problem.

The optimal partitioning of the graph is the one that minimizes the weights of the edges that were removed. A normalized cut criterion measures the dissimilarity between the different groups as well as total similarity within the groups. Here group size doesn't matter for normalized cut criterion. The normalized cut can be computed using three different splitting points and the result is analysed accordingly. A common approach for detecting the object from a video is to perform background subtraction, which identifies moving objects from the portion of a video frame that differs significantly from a background model and then apply the segmentation algorithm to that video. Here background subtraction has been done by frame difference method. In this method previous frame is subtracted from the current frame and difference is compared with the specific threshold value. For experimental purpose, videos of different flowers and movement of the tennis balls have been taken. All the experiments have been performed on both gray scale image and videos in MATLAB.

Author: Parekh, Devang (200811038)

Title: Implementation of High Speed Serial Communication Blocks; 39 p.; 2010.

Supervisor: Dubey Rahul
Call No.: 004.64 PAR
Acc. No.: T00270
Keywords: Microcomputers -- Buses; Universal Serial Bus; USB (Computer bus); Computer architecture; UTMI; High-Speed Clockless Serial Link Transceiver; Exchaning data; Data transmission

Abstract: Serial communication is widely being used from PCs to handheld mobile phones due to very less hardware, low cost, easier design process in comparison to parallel communication. For bit by bit, reliable transmission and receiving at the physical layer it is important for data sequences to have high transition density, low power spectral density, less bit error and reduced bandwidth. This thesis implements the universal serial bus 2.0 (USB 2.0) transceiver Macro cell interface (UTMI) in a generic form to use different low level signaling protocol blocks in other serial communication standards. The code written is synthesizable and verified for correct functionality. The HDL code is a state machine (Mealy machine) implementation from the specification of UTMI. The challenging part of the work was to implement clock and data recovery block as it involved a lot of engineering concepts like control theory, digital electronics and analog circuits. The work presents intricacies in the design of PLL for recovery of clock and data. UTMI helps in faster development of ASIC and provides an abstraction layer for the peripheral developers who are not involved in low level details of physical layer. Finally the results for UTMI implementation are presented.

Author: Patel, Amit (200811023)
Title: Relaization of FPGA-based Digital Controller; 33 p.; 2010.
Supervisor: Dubey, Rahul
Call No.: 621.395 PAT
Acc. No.: T00259
Keywords: Field programmable gate arrays -- Design and construction; Integrated circuits; Motion control devices; Digital electronics; Logic design; Computer architecture; Integrated circuits -- Fault tolerance

Abstract: Field Programmable Gate Array (FPGA) can be used to enhance the efficiency and the flexibility of digital controller. FPGA implementation of digital controllers leads to real time realizations with small size and high speed. Also it offers advantages such as complex functionality, fast computation, and low power consumption for high volume production. This thesis presents realization of FPGA based speed control of brushless dc (BLDC) motor - a real time application. The construction and the operation of the BLDC motor are described. The different control strategies for speed controller and digital pulse width modulation (PWM) control technique are implemented and tested on BLDC motor. Also their performance is evaluated. Proportional Integral (PI) controller and Fuzzy Logic Controller (FLC) are implemented in FPGA as a digital controller. The PI controller is governed by the values of proportional gain and integral gain, while FLC behaves in much similar way as human controls the system. Logics of both controllers: PI controller and fuzzy logic controller are written in High Description Language (HDL). The performance of the PI controller is better than the fuzzy logic controller in case of the complete known plant.

Author: Patel, Birenkumar (200811017)
Title: Transaction based Verification of Discrete Wavelet Transform IP core using Wishbone Transactor; 62 p.; 2010.
Supervisor: Dubey, Rahul
Call No.: 621.381548 PAT
Acc. No.: T00253
Keywords: Integrated circuits – Verification; Computer software – Verification; System design; Electronic circuits – Testing; Digital electronics; Electronic apparatus and appliances – Testing.

Abstract: Verification is major concern in product development life cycle. The number of human hours required writing a test bench and choice of verification approach is the major contributor in the

Non Recurring Engineering (NRE) cost. There are too many techniques for verification. Register Transfer level (RTL) verification is too slow. Transaction based verification technique is used for faster verification of any Intellectual Property core. Transaction-based verification allows simulation and debug at the transaction level, in addition to signal or pin level. All possible transaction types between different modules in a system are created and systematically tested. It does not require detailed test benches with large vector.

Device under test (DUT) operates at a binary stimulus level(e.g. Zeros and Ones). Test bench includes one model to define the transactions at a high level (e.g. READ) and another model to interpret transaction and translates them into the binary level. DUT is implemented in lower abstraction language like Verilog and test bench is created in higher abstraction language like C++.

The Discrete Wavelet Transform's (DWT) Intellectual Property (IP) core is used as a DUT. DWT is implemented by Lifting scheme based Daubechies 9/7 filter. Lifting scheme has an advantage over conventional convolution method like time complexity of operation. Wishbone transactor is designed for verification of IP core. Whole system is verified on ZeBu emulator. The same Wishbone transactor is used for verification of different Wishbone compatible IP core.

Author: Phophalia, Ashish (200811032)

Title: Classification of 3D Volume Data Using finite Mixture Models; 48 p.; 2010.

Supervisor: Mitra, Suman K.

Call No.: 006.693 PHO

Acc. No.: T00266

Keywords: Three-dimensional imaging -- Industrial applications; Computer graphics; Photography -- Digital techniques; Image processing -- Digital techniques; Three-dimensional imaging in medicine; Diagnostic Imaging

Abstract: The 3D imaging provides better view of objects from three directions as compared to 2D imaging where front face of object can be viewed only. It involves a complex relationship as compared to 2D imaging and hence computationally expensive also. But it also includes more information which helps in visualizing the object, its shape, boundary similar to real world phenomenon. The segmentation method should take care of 3D relationship that exists between voxels. The multi channel 3D imaging provides exibility in changing voxel size by changing echo pulse signals which helps in analysis of soft tissues. The application of 3D imaging in MRI brain images help in understanding more clearly the brain anatomy and function.

Mixture model based image segmentation methods provide platform to many real life segmentation problems. Finite Mixture Model (FMM) segmentation techniques have been applied in 2D imaging successfully. But these methods do not involve spatial relationship among neighboring pixels. To overcome this drawback, Spatially Variant Finite Mixture Model (SVFMM) was given for classification purpose. In the medical imaging, the probability of noise is high due to environment, technician expertise level, etc. So, a robust method is required which can reduce the noise effect of the images. The Gaussian Distribution is more preferred in the literature but it is not robust against the noisy data. The Student's t Distribution uses Mahalanobis squared distance to reduce the effect of outlier data. A comparative study has been presented between these two distribution functions.

In Medical Imaging, segmentation procedures provide facility to separate out different type of tissues instead of manual processing which requires time and efforts. The segmentation methods automate this classification procedure. To reduce the computation time in 3D medical imaging, a sampling based approach called Column Sampling is used. The variance of a column is taken as a measure in sample selection. A comparison is presented for time taken in sample selection from whole volume with Random Sampling. The selected samples are provided to the estimation technique. The parameters of mixture model are estimated using Maximum Likelihood Estimation and Bayesian Learning Estimation in the presented work. The method for estimating parameters of SVFMM using Bayesian Learning is proposed. The Misclassification Rate (MCR) is used for quantitative measure among these methods.

This work analyzes FMM and SVFMM models with different probability distribution over two

different estimation techniques. The MCR and computational time are considered as quantitative measures for performance evaluation. The different sampling percentage is tried out to estimate the parameters and their MCR and computational time are presented. In conclusion, Bayesian learning estimation SVFMM using Student's t distribution gives comparatively better results.

Author: Rajput, Nitin Singh (200811005)
Title: Game Theory Based Strategies for Cooperation in Ad Hoc Wireless Networks; 65 p.; 2010.
Supervisor: Srivastava, Sanjay and Divakaran, Srikrishnan
Call No.: 621.38216 RAJ
Acc. No.: T00245
Keywords: Wireless communication systems; Wireless LANs; Sensor networks; Wireless communication systems; Computer network architectures; Routers (Computer networks); Wireless communication systems -- Design and construction, Contrite; Game theory; Generosity; Nash equilibrium; Operating point; Optimality; Tit for tat (TFT).

Abstract: In self-organized ad-hoc wireless networks, nodes belong to different authorities, pursue different goals, have constrains like energy; therefore, cooperation among them cannot be taken for granted. Non cooperation of nodes causes increase in probability of packet drop and increase in probability of route or network failure, which leads to poor network performance. On other hand if nodes always cooperate, network does not last for a long as nodes are energy constrained. Several schemes are proposed in literature based on incentive and reputation mechanism. All of them outperforms in their own set of assumptions and have certain issues.

Researchers started looking at game theory as a probable solution and proposed some schemes, but yet to come up with better solutions. We focus on optimization of service received by a node from network and delivered to network considering energy as constraint. We first derive the probability by which a node accept the relay request of other nodes based on energy constraint. Then apply game theory based schemes Generous Tit For Tat (GTFT), Neighboring GTFT (N-GTFT) and contrite Tit For Tat (C-TFT) for acceptance of relay requests; well known in economics, behavioral science and biology for cooperation. We find that all above mention scheme converges towards parato optimal values of service received and deliver to network in presence and absentia of noise in network. We find that when network has pair wise mixed strategies (any two from GTFT, N-GTFT and C-TFT) then also convergences remain same as it is for single strategy. But when there are 50% non cooperative nodes (Always Drops strategy), C-TFT is the dominating strategy. Also C-TFT copes up with 10% or more noise in the network as other strategy fail to do so, however they cope well with lesser amount of noise. At the end CTFT evolve as the dominating strategy when all strategies including Always Drops simulated under evolutionary method of comparison in noisy and noise free network. C-TFT out performs because it switches to mutual Tit For Tat after cooperating against fixed unilateral non cooperation from other nodes and also cope up with own unintentional defection caused by noise.

Author: Rathore, Hitesh (200811006)
Title: Channel Estimation in OFDM Systems; 55 p.; 2010.
Supervisor: Joshi, Manjunath V.
Call No.: 621.38216 RAT
Acc. No.: T00246
Keywords: Orthogonal frequency division multiplexing; Wireless communication systems; Wavelength division multiplexing; Orthogonalization methods

Abstract: Orthogonal frequency division multiplexing (OFDM) is not a new concept, but its receiver design has constant improvement. OFDM uses available spectrum efficiently and the system provides high data rates. Many standards such as Digital video broadcasting (DVB), Wireless local area network (WLAN), 3GGP LTE uses OFDM as standard. Most of the digital communication systems nowadays are wireless, where information bits are transmitted over a radio channel. These radio channels are generally multi path channel which cause inter symbol interference (ISI). To remove the effect of ISI from received signal equalization is done, which requires the channel impulse

response. A good channel estimation technique can reduce the complexity of equalizer by large factor. Channel estimation can be done by sending pilot symbols at regular interval and at the receiver the channel impulse response is estimated using these received pilot symbols.

In this thesis various pilot based channel estimators are studied. We propose a new channel estimator, which is based on regularized least squares method and uses some prior information of the channel. The performance of existing channel estimators and proposed channel estimator is compared. The criteria for performance are on the basis of mean squared error (MSE) and symbol error rate (SER). Various adaptive channel estimators are also studied. We also propose a new adaptive channel estimator, based on two-dimensional normalized least mean squared (NLMS) algorithm with variable step size. The performance of existing adaptive channel estimators is compared with the proposed adaptive channel estimator. Performance comparison is based on MSE and the bit error rate (BER).

Author: Shah, Milind (200811028)
Title: Investigation on Multi-Band Fractal Antennas for Satellite Applications; 85 p.; 2010.
Supervisor: Gupta, Sanjay
Call No.: 621.3824 SHA
Acc. No.: T00262
Keywords: Antennas (Electronics); Antennas (Electronics) -- Design and Construction; Antennas (Electronics) -- Testing; Wireless communication systems; Microwave circuits; Strip transmission lines; Frequency variation

Abstract: Remote sensing is a very important application of satellite communication. In remote sensing applications, multiple frequencies are utilized. Use of different antennas for different frequencies is a complex task and so use of single multiband antenna is desirable. Fractal geometries can be utilized to design single multiband antenna operating at various required frequencies which may be widely separated and non-harmonically related.

In this thesis fractal geometry concept has been utilized to achieve multiband and compact design. Here multifractal cantor geometry is used due to its simple construction and ease in tuning. In addition to multiband behavior, the antenna must provide sufficient bandwidth. Unfortunately the microstrip antennas are having very narrow bandwidth. There are other techniques to increase bandwidth such as aperture coupled structure or electromagnetically coupled structure. But these solutions result in the complex multilayer structure. To prevent this complexity and to increase bandwidth, monopole structure has been utilized. Usually for satellite communication 28 dB to 32 dB gain is required. To fulfill this requirement, an array using multiband element is also designed.

Author: Sharma, Nisha (200811041)
Title: Design of Digital Accelerometer Based Seismic Sensor Node; 59 p.; 2010.
Supervisor: Ranjan, Prabhat
Call No.: 621.3821 SHA
Acc. No.: T00273
Keywords: Antennas (Electronics); Antennas (Electronics) -- Design and Construction; Antennas (Electronics) -- Testing; Wireless communication systems; Microwave circuits; Strip transmission lines; Frequency variation

Abstract: The aim of Design of Digital Accelerometer based Seismic Sensor Node is to propose a design for wireless sensor network for exploring the sub-surface region of the moon by studying the seismic waves generated over there. As Moonquakes are less frequent and are smaller in scale than are earthquakes, we need a sensor network of high sensitivity that can live up to a longer period of time over which we can take necessary readings to study the sub-surface region of moon.

In the system proposed, four seismic sensor nodes are considered which need to be arranged in linear fashion over the surface of the moon with the help of rover. These nodes would collect data of the passive seismic events that takes place on the moon and transmit it to the base station so

that the information could be used by the Researchers/ Seismological officials for further studies.

The components of the sensor node include an accelerometer, Analog to Digital converter. A microcontroller would collect data from sensor and store it on data flash. The power requirements of the sensor node would be met by a battery. The base station of the system would be on rover and would be able to collect data through direct transmission from all the four nodes.

The system thus developed would be able to collect the seismic events over a life time of approx. 6months. The thesis discusses the hardware design and issues faced during the design with their solution. The prime emphasis of the design is on the miniaturization in the size, low weight and lower power consumption of the node.

Author: Sheikh, Parveen (200811019)
Title: High speed, low offset voltage CMOS Comparator; 53 p.; 2010
Supervisor: Parikh, Chetan
Call No.: 621.395 SHE
Acc. No.: T00255
Keywords: CMOS Comparators; Operational amplifiers -- Design and construction; Comparator circuits -- Design and construction; Metal oxide semiconductors, Complementary; Comparator; Sigma-delta ADC; Low power design.

Abstract: The Analog to digital converters are the key interface blocks between the continuous time domain and the discrete-time digital domain. The performance of high-speed data conversion and digital communication interfaces is generally limited by the speed and precision with which the function of comparison can be performed. Thus, comparator speed and precision play a vital role in high performance ADC's.

CMOS comparators suitable for integration in VLSI technologies have been successfully realized for audio frequency applications, such as analog - to-digital (A/D) converters. The speed and resolution of MOSFET comparators are typically limited by the inherent MOSFET characteristics of low trans-conductance and relatively large device mismatches. However, there are several techniques for dynamic offset cancellation, dynamic biasing, and analog pipelining which significantly improve the speed and resolution achievable in an MOS based comparator.

The thesis proposes a novel approach which minimizes the offset of pre-amplifier as well as the latch with increment in the speed of the comparator. The total offset thus referred back to the input is minimized and hence the pre-amplifier gain be relaxed.

The CMOS circuit is implemented in 0.18 µm technology and simulated in LT-Spice.

Author: Shiyani, Bhavin R. (200811009)
Title: Transmultiplexer Design Using Different Filters; 55 p.; 2010.
Supervisor: Chakka, Vijaykumar
Call No.: 621.3822 SHI
Acc. No.: T00247
Keywords: Adaptive filters -- Design and construction; Signal processing -- Digital techniques; Coding theory; Signals Processing; MATLAB; Electric filters, Digital; Signal processing -- Digital techniques -- Data processing

Abstract: Transmultiplexer is one of the applications of Filter banks, which is used to transmit many signals simultaneously through a single channel and so that to separate at receiving end. Design of transmultiplexer using prototype filters (low pass filters and band pass filters) has been studied and analysed with respect to complexity. Transmultiplexer design using complexity efficient polyphase structure has been studied and analysed in this thesis. In this thesis, different complexity efficient structures better than polyphase using CIC based structure, multistage CIC based structure, two stage CIC based decimator and multistage CIC based structure with compensator have been proposed. Performances of proposed structures are analysed (analysis of pass-band fluctuation, stop-band attenuation of each filter in transmultiplexer) in MATLAB

environment with different classes of input like speech and image. This thesis also considers complexity of proposed structures.

Author: Shripat, Abhishek Kumar (200811020)

Title: Multiresolution Fusion of Satellite Images and Super-Resolution of Hyper-Spectral Images; 46 p.; 2010.

Supervisor: Joshi, Manjunath V.

Call No.: 621.367 SHR

Acc. No.: T00256

Keywords: Image processing; Computer graphics; Image processing -- Digital techniques -- Mathematical models; Markov random fields; Fusion; Multisensor; Multiresolution; Particle swarm optimization.

Abstract: This thesis presents a model based approach for multi-resolution fusion of the satellite images. Given a high resolution panchromatic (Pan) image and a low spatial but high spectral resolution multi spectral (MS) image acquired over the same geographical area, the objective is to obtain a high spatial resolution MS image. To solve this problem, maximum a posteriori (MAP) - Markov random field (MRF) based approach is used. Each of the low spatial resolution MS images are modeled as the aliased and noisy versions of their high resolution versions. The high spatial resolution MS images to be estimated are modeled separately as discontinuity preserving MRF that serve as prior information. The MRF parameters are estimated from the available high resolution Pan image using homotopy continuation method. The proposed approach has the advantage of having minimum spectral distortion in the fused image as it does not directly operate on the Pan digital numbers. This method does not require registration of MS and Pan images. Also the number of MRF parameters to be estimated from the Pan image is limited as homogeneous MRF is used. The time complexity of the approach is reduced by using the particle swarm optimization (PSO) in order to minimize the final cost function. The effectiveness of the approach is demonstrated by conducting experiments on real image captured by Landsat-7 ETM+ Satellite.

This thesis also presents the Super-resolution of Hyper-spectral satellite images using Discrete Wavelet Transform based (DWT) learning. Given low resolution hyper spectral images and a data base consisting of sets of LR and HR textured images and satellite images; super-resolution of the hyper spectral image is obtained. Four hyper spectral test images are selected from 224 bands of hyper-spectral images through principal component analysis (PCA) technique. Using minimum absolute difference (MAD) criterion the best match wavelet coefficients are obtained. The finer details of test image are learned from the high resolution wavelet coefficients of the training data set. The inverse wavelet transform gives super resolved image corresponding to the test image. The effectiveness of above approach is demonstrated by conducting experiments on real Hyper-spectral images captured by Airborne Visible Infrared Imaging Spectrometer (AVIRIS).

Author: Singh, Harsh Verdhan (200811035)

Title: Adaptive Analog Line Driver Using Digital Tuning; 53 p.; 2010.

Supervisor: Sen, Subahjit

Call No.: 621.38153 SIN

Acc. No.: T00268

Keywords: Electronic circuit design; Self-tuning controllers; Digital-to-analog converter; Analog electronic systems -- Testing; Analogue Front-End Architecture; Data transmission systems; Analog design; CMOS line driver; High speed amplifier; Adaptive line termination; Online tuning; Large-Scale Nonlinear Optimization in Circuit Tuning

Abstract: Transmission lines are widely used for transmitting electrical signals. A line driver is a part of the analog front-end transmitter for wired line communication. It is a voltage buffer that provides the necessary output current to drive the small load impedance of a terminated transmission line. The adaptive line driver must adapt to the load impedance of a terminated transmission line for minimizing reflections. The main requirements of an adaptive line driver are good matching to the input impedance of the transmission line over process variations, high output swing, unity gain.

Existing adaptive line drivers use analog tuning methods for adapting to the load impedance. This thesis proposes a new technique for tuning output impedance of the line driver. A digital tuning method is used to correct the output impedance of the line driver to match with the input impedance of the transmission line. The aim of using the digital tuning method is to achieve better tuning range over existing analog tuning methods.

The tuning scheme uses a comparator followed by counter and current DAC(digital- to-analog converter). A comparator is used for comparing input and output signal of line driver and generates control signal which is applied to a counter that controls the current DAC. This feedback loop ensures unity gain between the input and out- put voltages and thereby ensures tuning of the output impedance of the line driver. The analog line driver is implemented in GPDK-180nm technology and simulated in Cadence Virtuoso Environment.

2010-2012

Author: Aghera, Piyush (201011011)
Title: An Approach to BuildMulti-Tenant SaaS Application With Monitoring and SLA
Supervisor: Chaudhary, Sanjay
Call No.: 006.78 AGH
Acc. No.: T00347
Keywords:
Abstract: SaaS (Software as a Service) is a modern approach to deliver large scalable enterprise software as a service on Internet. Cloud computing platform provides the scalability, availability and utility computing for services on internet. There are many technical challenges involved in SaaS development. One of them is multi-tenancy, which allows single instance of software to serve multiple organizations by accommodating their unique requirements through conguration at the same time. SaaS architecture requires both conguration and some level of customization to achieve higher maturity model. In this thesis, we propose a metadata based SaaS application architecture which is independent of underlying cloud infrastructure. We aim to propose independent SaaS platform concepts, to avoid vendor locking as observed in case of many commercial service providers. SaaS application development should be independent of underlying infrastructure so that application can be migrated from one cloud to another cloud without changing the code. It is possible only if all the players follow the identical as well dened standard SaaS architecture. Our proposed architecture includes monitoring, tenant management, tenant administration, tenant conguration and large data management services. Existing architecture has used simple XML le to store and retrieve tenant specic conguration. File operations are the bottle neck while accessing data for large organization at the same time. In this approach, we have used Memcached concept and it is supported by almost all databases to boost the performance. In addition to this, we have considered application pooling on a web server to manage priority among tenants. Application pooling works as a static load balancer for incoming large request. To realize proposed architecture, we have developed and demonstrated seleced functionalities of University Management System and it is capable to support multi-tenancy.

Author: Agrawal, Amit H. (201011020)
Title: Forward Error Correction for Software Defined Radio based on FPGA
Supervisor: Dubey, Rahul
Call No.: 621.38224 AGR
Acc. No.: T00355
Keywords:
Abstract: In digital communication, the signal to noise ratio (SNR) of the channel is one of the major limitations on the operating performance. Solution in terms of coded data and error-correcting code has been introduced to improve the performance. Forward error correction technique with Convolution encoding and Viterbi decoding has been introduced here for this purpose. A Convolution encoder and Viterbi decoder of code rate 1/2, constraint length (K) of 7, 8 & 9 has been designed using Verilog HDL and incorporated with our application Software defined radio using black box in MATLAB Simulink. It is important to improve the performance and reduce the power and area of the decoder. In this project, Viterbi decoder adopted the Process Element (PE) technique which made it easy to adjust the throughput of the decoder by increasing or decreasing the number of PE. By the method of Same Address Write Back (SAWB), the number of registers reduced to half in contrast with the method of ping-pong.

Author: Agrawal, Rupesh (201011022)

Title: Traffic Driven Topology Control For Network Lifetime Maximization
Supervisor: Srivastava, Sanjay and Muthu, Rahul
Call No.: 621.382 AGR
Acc. No.: T00357
Keywords:
Abstract: Energy consumption is a major concern in ad hoc wireless networks. Network life-time can be maximized by minimizing the network power consumption. Topology control is one of the most important mechanisms used for reducing network power consumption. Topology control can be achieved either by transmit power control or sleep scheduling. In transmit power control the optimization problem is to find the transmission power at which the power consumption is minimized while maintaining desired connectivity. In sleep scheduling, nodes which are redundant are switched on and off using a scheduling algorithm. One of the main problem with sleep scheduling is whenever the traffic pattern changes, path going through awake nodes may become longer while there may exist a shorter path considering some of the sleeping nodes. This will increase per packet transmission energy consumption as well as end to end delay. In this thesis we propose a traffic aware topology control protocol to solve this problem. It finds out subset of sleeping nodes to be awakened on the basis of current traffic scenarios so that total traffic weighted network cost can be minimized at global level hence saving the overall energy of the network and maximizes the network life- time. Simulation results show that,our proposed protocol is able to save a signicant amount of energy while maintaining end to end packet delay.

Author: Ambasana, Nikita B.
Title: FPGA Implementation of Environment/Noise Classification Using Neural Networks
Supervisor: Zaveri , Mazad S.
Call No.: 006.32 AMB
Acc. No.: T00362
Keywords:
Abstract: The purpose of this thesis is to give an insight into the implementation of a system of neural networks, for the tasks of Noise/Environment Modeling, Feature Extraction and Classification of Noise/Environment, on a Field Programmable Gate Array (FPGA). A methodology for creating baseline architecture for a new system of neural networks has been followed, to give worst case estimates. After necessary analysis an estimate of hardware utilization, within a specific FPGA (XC3S250E Spartan 3E Device) and the Time for Computation, for each of the machines used, is given. It also summarizes the Performance-Price Ratio in terms of Time of Computation and Hardware for Logic simplementation, for different degrees of parallelism in the system.

Author: Basha, Shaik Mahaboob (201011048)
Title: Improvement of RAD Technique for Detecting Reflector based DoS Attack
Supervisor: Mathuria, Anish
Call No.: 005.8 BAS
Acc. No.: T00372
Keywords:
Abstract: Distributed Reflector Denial-of-service (DRDoS) attack is a challenging problem in present Internet environment. DRDoS attack is entirely different when compared to DDoS attack. In DRDoS attack, no need to generate the huge amount of traffic by attacker. Attacker can initiate the multiple compromised hosts (zombies), they will generate the request traffic. The innocent reflector generates the attack traffic. But from victim point of view it is very difficult to find the attacker and attack traffic because actual attacker hides behind the legitimate reflector. Many prevention systems have been proposed in DRDoS attack. All prevention techniques have false negatives and false positive. Among all, Reflector Attack Defense (RAD) technique is efficient one. But RAD technique has few limitations like replay attack and passing the false request packets by core router. In this thesis work we enhance the RAD technique in such a way that it will perform successful differentiation between the legitimate traffic and attack traffic. Not only this, all previous proposals are only compatible with IPv4 only. They are not compatible with IPv6. Science IPv6 is usually to see widespread

deployment in the future; we seek a solution that is also compatible with IPv6. So enhanced prevention system will filter the DRDoS traffic efficiently and also work with IPv6. This thesis shows the two different techniques to filter the attack traffic. One is filtering the attack traffic at the client edge router; another one comes when the local filtering cannot handle the huge attack traffic. Second technique filters the traffic at core of Internet by marking the packets at Autonomous System level.

Author: Bhumireddy, Venkata Ratnam (201011012)
Title: Design of Low Power and High Speed Comparator with DG-MOSFET
Supervisor: Sen, Subhajit
Call No.: 621.3815284 BHU
Acc. No.: T00348
Keywords:
Abstract: This thesis is about design of low power and high speed comparator with Double Gate- Metal Oxide Semiconductor Field Effect Transistor (DG-MOSFET) in 32 nm technology node. Low power is the requirement in implanted biomedical devices which consists of data converters. Low power and high speed is the important parameter in signal processing which consists of data converters. Hence power and speed became a critical parameter to optimize in data converters and memory applications to increase the battery life by reducing its energy consumption. Here, this dissertation describes a dynamic comparator which can be operated with a clock frequency of 3.5 GHz. It takes delay of 35.12 ps, an average power of 6.19 □W in reset phase and 8.16 □W in comparison phase at a clock frequency of 1 GHz. The external positive feedback uses the multi-vt property of DG-MOSFET that is the dependence of rst gate voltage on second gate bias voltage, to reduce the regeneration time.

Author: Chavada, Sujit Dilipkumar (201011045)
Title: FPGA Based Platform for Spiking Neural Networks
Supervisor: Zaveri, Mazad
Call No.: 006.32 CHA
Acc. No.: T00371
Keywords:
Abstract: Neuromorphic engineers are studying the nervous system and trying to emulate its function and organization in their computational and robotics systems. They are hoping to match the human brain in vision, hearing, pattern recognition and learning tasks. Our goal is to create Field Programmeble Gate Array (FPGA) platforms of large-scale spiking neural networks to allow the testing of certain hypotheses related to neuroscience theories. Virtualization is also very important concept for spiking neural network. In this work, we also analyze effect of virtualization on performance and performance/price of spiking neural network. We implement general purpose spiking neural network platform using Spartan 3E FPGA and observe performance and performance/price tradeoffs.

Author: Chhaya, Vaibhav (201011009)
Title: CMOS Current-based Mixed-Signal Architecture for Vector-Matrix Multiplication
Supervisor: Zaveri , Mazad S.
Call No.: 621.39732 CHH
Acc. No.: T00345
Keywords:
Abstract: In present days electronic devices become faster. Computations like vector matrix multiplication become more and more compliant and lengthy. For that CMOS based vector-matrix multiplication architecture, with external digital interface and internal current-based analog operation is presented here. The basic circuits within this architecture are: a binary multiplier that contains a static memory, a current source, a current accumulator and current-to-voltage convertor. The external operand arrives sequentially, so a serial-to-parallel shift-register memory is also implemented. In LTSpice, using 180nm CMOS technology, I have implemented a vector-matrix multiplier circuit that simultaneously performs 64×4 binary multiplications.

Author: Gondaliya, Khushal V. (201011024)
Title: Zero-Aware 6T Asymmetrical SRAM Cell for Low Power Cache Application
Supervisor: NagChoudhuri, Dipankar
Call No.: 621.39732 GON
Acc. No.: T00358
Keywords:
Abstract: enjoyed many conversations in the lab with the friends, which was useful to improve my work significantly. I would like to thank my hostel friends Piyush, PG, Ajay, Shyam, Hirav, Vishal, Jaykant, Sujit and Yash for the great discussions that we had in the hostels which made me refresh every time during tense and tired period. I am especially grateful to Tanvina Patel, for her kind help in editing of my document. Thanks to my all friends on campus and outside, I have a many memorable moments with them outside my work. At last a word of thanks also to my HP Pavilion dv2000, along with heartiest thanks to my parents and Lord without which it would be very difficult for me to complete any of my task effectively.

Author: Jain, Shefali (201011037)
Title: Enhancement of Misbehavior Detection Scheme for Vehicular Ad-hoc Networks
Supervisor: Mathuria, Anish
Call No.: 005.8 JAI T00367
Acc. No.: T00367
Keywords:
Abstract: Vehicular ad hoc networks (VANETs) will facilitate various safety and non-safety applications to be deployed in the future. A vehicle in a VANET can misbehave by sending false or inaccurate information to other vehicles. Detection of such misbehavior is an important research problem. In this thesis, we study and improve an existing scheme for misbehavior detection. In that scheme, if a vehicle X generates an incorrect alert, then the nearby vehicles report the misbehavior of X to Road side unit (RSU). Upon receiving such a report, RSU imposes a fine on vehicle X. It is possible for a malicious vehicle to send a false report implicating X, even if X has generated a correct alert. As a result, the RSU may inadvertently fine an honest vehicle, potentially discouraging it from sending true alerts in the future. In this thesis, we propose a modified RSU detection algorithm to avoid honest vehicles from being fined due to malicious reports. We perform a simulation of the modified scheme and show that it identifies misbehaving vehicles with high accuracy.

Author: Jain, Yash (201011035)
Title: Generating Recommendations For Agricultural Crop Production
Supervisor: Chaudhary, Sanjay
Call No.: 633.5191 JAI
Acc. No.: T00365
Keywords:
Abstract: Agricultural Productivity depends on large number of parameters such as climatic conditions, soil quality, socio-economic factors, cultural practices, cultivation factors, technological innovations etc. The change in climate has a significant impact on the crop production. Scientists all over the world are trying to model the change in climate and various parameters affecting it. A huge amount of spatial data is available regarding climatic conditions, agricultural productivity etc. The data is available at varying resolutions. Applications of spatial data analysis in generating the rec-ommendations for farmers is considered. We specifically consider for cotton crop in North Gujarat region. A recommendation system is developed which helps farmers in various stages of farming. An extensive knowledge base in the form of ontology is also developed to provide support for better reasoning. The future extensions of the work includes the development of web based interfaces and a service oriented architecture to access the system in a platform independent manner. The recommendations would typically help the farmers choose the appropriate fertilizers, pesticides, cultural methods etc.

Author: Joshi, Priyanka (201011003)
Title: Agro-produce Marketing: Development of Agro-tagger and Suggestion Generation System
Supervisor: Chaudhary, Sanjay
Call No.: 381.41 JOS
Acc. No.: T00341
Keywords:
Abstract: The growing use of internet has developed interest in the eld of Information Extraction. Most of the documents on internet are unstructured text that can be structure dusing information extraction techniques. Social Networking sites play a prominent role in the life of people by providing a platform, that allows users to share ideas, activities, events, and interests. Social networking sites have a great marketing potential that can be exploited in Agro-produce marketing domain. The farmers and merchants can post about their interests. These tweets are be analyzed and suggestions can be generated for both farmers and merchants. A domain specic information extraction system is developed for Agro-produce marketing domain for extracting entities crop name, variety, price, quantity, location and deadline from the web. The text engineering framework - General Architecture for Text Engineering (GATE) provides ANNIE, an information extraction plug-in, which is extended and modied for building the system. The core of the system is based on pattern action grammar rules. The Agro-tagger identies the entities related to agro-produce marketing from a given document and tag them.

Author: Joshi, Srawan Kumar (201011008)
Title: A Novel 7T SRAM cell design for Low Power Cache Applications
Supervisor: Nagchoudhuri, Dipankar
Call No.: 621.397 JOS
Acc. No.: T00376
Keywords:
Abstract: Scaling in integrated circuit technology directly paves way to increased package density, thereby increasing onchip power. With continuous scaling, low power design techniques results in efficient use of silicon die. Semiconductor memories are most important subsystems of modern digital systems. Modern IC's allocate 70% of the total chip area to memory design. SRAM is used as on chip cache memory. A major part of the power consumption in any memory architecture is due to charging and discharging of highly capacitive bitlines and wordlines. Existing techniques mainly concentrated on the reduction of power due to the capacitive bitlines and wordlines. In this thesis, a new 7T SRAM cell has been proposed with a single bitline architecture which reduces the dynamic power consumption to a great extent. This proposed design resulted in power reduction of write '0' and read '0' operation, based on the fact that the majority of the cache writes are 0's. A memory array of size 256Kb (512x512) was designed using the basic 6T SRAM and propsed 7T SRAM cell to carry out the simulations and compare the results for power optimization. The simulations were done using Cadence Virtuoso (ADE) tool in gpdk180 library using 0.18µm technology. With the proposed SRAM cell implementing 256Kb memory array, reduction of write power (approximately 80%) and read power (approximately 55%) is achieved compared to conventional SRAM array. There is an area overhead of 28.76% using the present 180nm technology.

Author: Kotecha , Shyam (201011015)
Title: SQL-GQL Inter-Query Translation For Google App Engine Datastore
Supervisor: Bhise, Minal
Call No.: 006.78 KOT
Acc. No.: T00350
Keywords:
Abstract: On demand services, usage based pricing, and scalability features of cloud computing has attracted many customers to move their applications into cloud. But different cloud service providers are using different standards & frameworks to host applications & data. Customers have to follow these standards and frameworks. When customer wants to migrate application

and/or data to another cloud service provider, application code and database structure must be modified according to the standard of new cloud service provider. This modification is very costly and as a consequence, changing cloud service provider becomes difficult. This situation is called vendor lock-in in cloud. Focusing on database, complete database migration requires migration of data, database schema, and query. This thesis work concentrates on migration of query. Automation in migration process is achieved by translation algorithms. This thesis work introduces inter-query translation algorithms. These algorithms translate SQL (Structured Query Language) query and GQL (Google Query Language) query into each other. The implementation of these algorithms is demonstrated for MySQL Sakila database.

Author: Mandloi, Dipendra Singh (201011013)
Title: SPARQLGen: Generation of SPARQL from Pseudo BGP
Supervisor: Chaudhary, Sanjay and Jat, Pokhar Mal
Call No.: 006.78 MAN
Acc. No.: T00349
Keywords:
Abstract: SPARQL is the querying language and communication protocol for communicating with RDF data sources. SPARQL query requires knowledge of URIs of bound values in the triple patterns and ontological schema used by dataset. A person, even expert in SPARQL, nds hard to gure out URIs for bound values to be used in the query. This requirement brings a gap between end user and SPARQL query formation. In this work, we aim to facilitate semantic search over web of data by converting keywords into URIs, and present SPARQLGen. SPARQLGen provides an easy way of writing SPARQL query for a given query over Web of Data (RDF data). Through appropriate interface, semantic annotations of keywords are captured. We derive a Pseudo Basic Graph Pattern which is basically similar to SPARQL BGP except that it contains keywords rather than full resource URIs. Here, we propose heuristics that discover URIs for annotated keywords and build corresponding SPARQL query. SPARQLGen takes services of falcons, a semantic search engine. The Linked Open Data plays the major role in nding aliased URIs of an entity. The nal set of results contains a list of URIs of different data sources. SPARQLGen bridges the gap between end user and SPARQL query formation. The interface allows users to write user intended keywords instead of highly syntactic SPARQL query so that he/she needs not worry about the URIs of entities while writing their queries.

Author: Munshi, Paridhi (201011042)
Title: Fingerprint Image Preprocessing for Robust Recognition
Supervisor: Mitra, Suman K.
Call No.: 621.367 MUN
Acc. No.: T00369
Keywords:
Abstract: Fingerprint is the oldest and most widely used form of biometric identification. Since they are mainly used in forensic science, accuracy in the fingerprint identification is highly important. This accuracy is dependent on the quality of image. Most of the fingerprint identification systems are based on minutiae matching and a critical step in correct matching of fingerprint minutiae is to reliably extract minutiae from the fingerprint images. However, fingerprint images may not be of good quality. They may be degraded and corrupted due to variations in skin, pressure and impression conditions. Most of the feature extraction algorithms work on binary images instead of the gray scale image and results of the feature extraction depends upon the quality of binary image used. Keeping these points in mind, image preprocessing including enhancement and binarization is proposed in this work. This preprocessing is employed prior to minutiae extraction to obtain a more reliable estimation of minutiae locations and hence to get a robust matching performance. In this dissertation, we give an introduction to the ngerprint structure and identification system . A discussion on the proposed methodology and implementation of technique for fingerprint image enhancement is given. Then a rough-set based method for binarization is proposed followed by the discussion on the methods for minutiae extraction. Experiments are conducted on real

fingerprint images to evaluate the performance of the implemented techniques.

Author: Nair, Rahit R. (201011036)
Title: Aplication of Compressive Sensing to Two-Way Relay Channel Estimation
Supervisor: Chakka, Vijaykumar
Call No.: 621.382 NAI
Acc. No.: T00366
Keywords:
Abstract: An Amplify and Forward Two-Way Relay Network is one where two nodes transmit data to each other via an intermediate relay. The relay amplifies the superimposed data from both the nodes before sending it to both the nodes. A method for the estimation of channel is proposed for Amplify and Forward Two-Way Relay Network (AF-TWRN). The proposed method utilizes the fact that the channel in the case of AF-TWRN shows sparse characteristic. The sparse multipath channel is estimated in the case of AF-TWRN using compressive sensing (CS) reconstruction algorithm, namely Iterative Hard Thresholding (IHT). MSE based performance of these methods in estimating the composite AF-TWRN channel was calculated and compared to that using Compressive Sampling Matching Pursuit (CoSaMP) and Orthogonal Matching Pursuit (OMP). IHT and CoSaMP are seen to perform slightly better than OMP with lesser computational complexity than OMP. It was also shown that all three CS based estimation methods perform better than the traditional Least Squares (LS) method in the estimation of Sparse AF-TWRN channel. A low complexity detection strategy was proposed

Author: Padiya, Trupti (201021006)
Title: Semantic Web Data Management: Data Partitioning and Query Execution
Supervisor: Bhise, Minal
Call No.: 025.0427 PAD
Acc. No.: T00375
Keywords: Data Partitioning, Materialized View, Query Performance, Scalability, and Semantic Web.
Abstract: Semantic Web database is an RDF database. Due to increased use of Semantic Web in real life applications, we can find immense growth in the use of RDF databases. As there is a tremendous increase in RDF data, efficient management of this data at a larger scale, and query performance are two major concerns. RDF data can be stored using various storage techniques. The RDF data used for this experiment is FOAF dataset which is a social network data. Here we study and evaluate query performance for various storage techniques in terms of query execution time and scalability using FOAF data set. Thesis demonstrates effect of data partitioning techniques on query performance. For our experiments, we have used Triple Store, Property Tables, vertically and horizontally partitioned data store to store FOAF data. Experiments were performed to analyze query execution time for all these data stores. Partitioning techniques have been observed to make queries 168 times faster compared to Triple Stores. Materialized views are used to improve query performance further for the queries which are seen frequently for social web data. Materialized views have shown better query performance in terms of execution time which is 8 times faster than the partitioned data.

Author: Pariyani, Sandeep (201011017)
Title: Design of an Analog Phase Shifter at X-band for Radar and Telecom Applications
Supervisor: Gupta, Sanjeev
Call No.: 621.3815 PAR
Acc. No.: T00352
Keywords:
Abstract: When examining a monthly bank account statement it is not only the number below the bottom line that matters. Whether that number has a minus or plus in front of it is also crucial. For many technical issues, the sign matters as well. In circuits, we can change the sign of the RF signal by means of phase shifters. Moreover, by using phase shifters, intermediate states between the signs (including complex values) can be set in circuits With

the increasing use of wireless systems in GHz range, there is high demand for integrated phase shifters in phased arrays and MIMO on chip systems. An analog phase shifter has been designed and analyzed to meet the needs of Radar and Telecom applications. An X-band (8-12 GHz) analog phase shifter using vector modulator principle is designed and analyzed using microstrip planar trans- mission line. The output of phase shifter at 0, 10, 45, 90, 135 and 180 has phase error in the range of □5. The input return loss is in the range of 5-7 dB and the output return loss is in the range of 5-15 dB. Also the insertion loss of the designed phase shifter is in the range of 5-8 dB. The designed phase shifter is then compared with commercially available Hittite's analog phase shifter.

Author: Parmar, Ajay (201011032)
Title: Person Identification using Face and Speech
Supervisor: Joshi, Manjunath V.
Call No.: 006.4 PAR
Acc. No.: T00363
Keywords:
Abstract: In this thesis, we present a multimodal biometric system using face and speech features. Multimodal biometrics system uses two or more intrinsic physical or behaviour traits to provide better recognition rate than unimodal biometric systems. Face recognition is built using principal component analysis (PCA) and the Gabor filters. In Face recognition, PCA is applied to Gabor filter bank response of the face images. Speaker recognition is built using amplitude modulation - frequency modulation (AM-FM) features. AM-FM features are weighted-instantaneous frequency of the analytical signal. Finally, weighted sum of score of face and speaker recognition system is used for person identification. Performance of our system is evaluated by using ORL database for face images and ELSDSR database for speech. Experimental results show better recognition rate for the multimodal sytem when compared to unimodal system.

Author: Patel, Chirag R. (201011018)
Title: Person Identification from their Hum with Inter-session Variability Compensation
Supervisor: Patil, Hemant
Call No.: 006.454 PAT
Acc. No.: T00353
Keywords:
Abstract: In this thesis, design of person recognition system from their hum is discussed. The emphasis is given to the inter-session variability of the recognition system. Standard database is not available for the inter-session variability of humming-based person recognition systems. Therefore, humming database of 50 subjects is collected in two training and six testing sessions. The MFCC (Mel Frequency Cepstral Coefficients) is the state-of-the-art feature set in the field of speech and speaker recognition systems. In this thesis, another cepstral feature viz., VTMFCC (Variable length Teager energy based MFCC) is used along with MFCC. VTMFCC captures the vocal source information. Two modulation-based features, viz., AM-FM and Q-features are introduced in this thesis. The performance of all of the four features in multi-session environment is evaluated using discriminately-trained polynomial classifier. Polynomial classifier uses out-of-class information while creating person- specific person model. Inter-session variability degrades the performance of person recognition systems due to difference in training and test sessions. This variability can be classified as intrinsic variability and extrinsic variability according to its source of origin. Inter-session variability due to speaker's health, aging, emotional state, etc. is called intrinsic inter-session variability. The session variability due to environment conditions, noise, change in microphone and acoustic channel is called extrinsic inter-session variability. The inter-session variability degrades the performance of all four features, i.e., MFCC, VTMFCC, AM-FM and Q-feature. The difference in % EER (Equal Error Rate) of particular test session to base test session is used as the inter-session variability measure. The base test session is a test session which is collected with the training session. In this thesis, two new approaches have been proposed for the compensation of inter-session variability, viz., feature-level fusion and model-level fusion. These two approaches reduce the degradation in the performance of

person recognition system due to inter-session variability and make the system robust.

Author: Radadia, Purushotam G. (201011050)
Title: Feature Based Approach for Singer Identification
Supervisor: Patil, Hemant A.
Call No.: 006.454 RAD
Acc. No.: T00374
Keywords:
Abstract: One of the challenging and difficult problems under the category of Music Information Retrieval (MIR) is to identify a singer of a given song under strong instrumental accompaniments. Besides instrumental sounds, other parameters are also severely affecting Singer IDentification (SID) accuracy, such as quality of song recording devices, transmission channels and other singing voices present within a song. In our work, we propose singer identification with large database of 500 songs (largest database ever used in any of the SID problem) prepared from Hindi (Indian Language) Bollywood songs. In addition, vocal portions are segmented manually from each of the songs. Different features have been employed in addition to state-of-the-art feature set, Mel Frequency Cepstral Coefficients (MFCC) in this thesis work. To identify a singer, three classifiers are employed, viz., 2nd order polynomial classifier, 3rd order polynomial classifier and state-of-the-art GMM classifier. Furthermore, to alleviate the effect of recording devices and transmission channels, Cepstral Mean Subtraction (CMS) technique on MFCC is utilized for singer identification and it is providing better results than the baseline MFCC alone. Moreover, the 3rd order classifier outperforms amongst all three classifiers. Score-level fusion technique of MFCC and CMSMFCC is also used in this thesis and it improves the results significantly.

Author: Rana, Kunj (201011004)
Title: Study of the Effectiveness of Various Low Power Techniques on Sequential and Combinational Gate Dominated Designs
Supervisor: Bhatt, Amit
Call No.: 621.395 RAN
Acc. No.: T00342
Keywords:
Abstract: In last decade, the technological advancement is seen in semiconductor field like never before. The need for low power has caused a major paradigm shift where power dissipation has become as important consideration as performance and area. The size of the electronic equipments is getting smaller and smaller which requires smaller integrated circuits (ICs). Due to this the power consumption happens to be a major concern in developing the smaller ICs. The objective of the dissertation is to develop a low power digital design flow using Cadence® tools. This report discusses various strategies and methods for designing low power circuits and systems. It describes the many issues facing designers at various levels and presents some of the techniques that have been proposed to overcome these difficulties. To do this, particular RTL (Verilog code) is taken for some design. First various floorplans are tested on the design for better power number then using the same design, analysis on two different interconnect estimation model is done. Finally using the floorplan and interconnect estimation model analysis results low power implementation is done for the same design which is passed through various steps of digital design flow like synthesis, floor planning, placement, routing, and converted to GDSII (Graphic Database System) file format which can be directly sent to foundry. In low power implementation several techniques like clock gating, operand isolation, and multi Vt cells are used with some enhancement switches provided by the tool.

Author: Rao, D.Srinivas
Title: Analysis of Charge Injection in a MOS Analog Switch with impedance on Source side
Supervisor: Sen, Subhajit
Call No.: 621.398 RAO
Acc. No.: T00360

Keywords:

Abstract: Turning off of a transistor introduces error voltage at the output of Sample and Hold circuits which are the key components of Analog to Digital Converters (ADCs) and hence limits their accuracy of performance in high switching applications. The error voltage at output is mainly caused because of charge injection due to the carriers released from the channel and due to coupling through gate-to diffusion overlap capacitances. Hence, in order to fully understand the behaviour of charge injection in the presence of source impedance, a device is modelled and simulated in Pisces. This thesis is about modelling of an N-type Metal Oxide Semiconductor (NMOS) device in Pisces Postmini Tool with a hold capacitor on drain side, so that it can be used as a CMOS Analog switch. The main aim is to analyze the trends in output error voltage in the presence of source resistance. The output error caused due to charge injection is examined as a function of different parameters like gate voltage fall time, source resistance, input voltage, substrate concentration etc. Test structures similar to the one modelled in Pisces is simulated in 0.18µm CMOS technology for the verification purpose. It is shown that the modelled and simulated results exhibit good trend agreement.

Author: Shah, Hirav (201011010)
Title: Transaction Based Verification of Multimedia IP
Supervisor: Dubey, Rahul
Call No.: 621.381548 SHA
Acc. No.: T00346
Keywords:

Abstract: Verification is major concern in product development life cycle. The number of human hours required writing a test bench and choice of verification approach is the major contributor in the Non Recurring Engineering (NRE) cost. There are too many techniques for verification. Register Transfer level (RTL) verification is too slow. Transaction based verification technique is used for faster verification of any Intellectual Property core. Transaction-based verification allows simulation and debugging at the transaction level, in addition to signal or pin level. All possible transaction types between different modules in a system are created and systematically tested. Design under test (DUT) operates at a binary stimulus level (e.g. Zeros and Ones). Test bench includes one model to define the transactions at a high level and another model to interpret transaction and translates them into the binary level. DUT is implemented in lower abstraction language like Verilog and test bench is created in higher abstraction language like C++. The JPEG Encoder Intellectual Property (IP) core is used as a DUT. This IP is taken from opencores.org website. Whole system is verified on ZeBu emulator.

Author: Sharma, Amita (201011025)
Title: Reducing Climate Vulnerabilities of Cotton Farmers in Banaskantha (North Gujarat)
Supervisor: Chaudhary, Sanjay
Call No.: 633.5191 SHA
Acc. No.: T00359
Keywords:

Abstract: The multiple regression models is used to analyze the effect of frequently changing weather, like wide uctuation in monsoon rains, extremes in temperature, etc. on the cotton crop in North Gujarat Region. The study is basically focused on Banaskantha district of North Gujarat using data from 1991-2008. This study is conducted in two parts: (i) rst part contains analysis on monthly rainfall with respect to cotton yield and (ii) second part contains analysis based on different weather parameters like total seasonal rainfall, average temperature in degree days, relative humidity, and soil moisture with respect to cotton yield. Results from the statistical analysis are veried by the information collected from expert agronomists on cotton regarding different growth stages and different requirements of cotton in those growth stages.

Author: Sharma, Dushyant Kumar
Title: Reduction of Power Using Innovative Clock Gating & Multi Vth Techniques in Digital Design

Supervisor: Bhatt, Amit
Call No.: 621.395 SHA
Acc. No.: T00344
Keywords:
Abstract: Low power is one of the most important issues in today's ASIC (Application Specific Integrated Circuit) design. As the transistors scale down, power density becomes high and there is immediate need of reduction in power. There are different techniques available for reduction of power like Operand isolation (OI), Clock Gating (CG) and Multi Vth Library Utilization (MVLU). In this report, we present two approaches for power reduction. The first approach gives two algorithms that show how power and performance matrix is improved compared to conventional MVLU technique. In the second approach, it shows the implementation of constrained fanout clock gating and its benefits over conventional clock gating techniques in ASIC design methodology. This report also presents two analyses. The first analysis shows how the design metrics area, power and performance change due to different techniques of low power (Operand Isolation, Clock Gating and Multi Vth Cell Utilization). The second analysis demonstrates the effect of different CG cells in design and presents how the same design metrics are affected for each CG cell. There are two variations in each CG cell, one is with Reset and the other is without Reset. In this report, we also demonstrate how the design metrics are affected by insertion of Reset signal in each CG cell.

Author: Shikkenawis, Gitam (201011049)
Title: Locality Preserving Projection : A Study and Applications
Supervisor: Mitra, Suman K.
Call No.: 621.367 SHI
Acc. No.: T00373
Keywords:
Abstract: Locality Preserving Projection (LPP) is a recently proposed approach for dimensionality reduction that preserves the neighbourhood information and obtains a subspace that best detects the essential data manifold structure. Currently it is widely used for finding the intrinsic dimensionality of the data which is usually of high dimension. This characteristic of LPP has made it popular among other available dimensionality reduction approaches such as Principal Component Analysis (PCA). A study on LPP reveals that it tries to preserve the information about nearest neighbours of data points, thus may lead to misclassification in the overlapping regions of two or more classes while performing data analysis. It has also been observed that the dimension reducibility capacity of conventional LPP is much less than that of PCA. A new proposal called Extended LPP (ELPP) which amicably resolves two issues mentioned above is introduced. In particular, a new weighing scheme is designed that pays importance to the data points which are at a moderate distance, in addition to the nearest points. This helps to resolve the ambiguity occurring at the overlapping regions as well as increase the reducibility capacity. LPP is used for a variety of applications for reducing the dimensions one of which is Face Recognition. Face Recognition is one of the most widely used biometric technology for person identification. Face images are represented as high-dimensional pixel arrays and due to high correlation between the neighbouring pixel values; they often belong to an intrinsically low dimensional manifold. The distribution of data in a high dimensional space is non-uniform and is generally concentrated around some kind of low dimensional structures. Hence, one of the ways of performing Face Recognition is by reducing the dimensionality of the data and finding the subspace of the manifold in which face images reside. Both LPP and ELPP are used for Face and Expression Recognition tasks. As the aim is to separate the clusters in the embedded space, class membership information may add more discriminating power. With this in mind, the proposal is further extended to the supervised version of LPP (SLPP) that uses the known class labels of data points to enhance the discriminating power along with inheriting the properties of ELPP.

Author: Shinghal, Khushboo (201011034)
Title: SMS Query Processing for Information Retrieval
Supervisor: Majumder, Prasenjit
Call No.: 025.04 SHI

Acc. No.: T00364
Keywords:
Abstract: SMS text messaging is one of the fast and popular communication mode on mobile phones these days. This study presents a query processing system for information retrieval system when queries are Short-message-Service (SMS). SMS contains various user improvisation and typographical errors. Proposed approach uses approximate string matching techniques and context extraction to normalize SMS queries with minimum linguistic resources. We have tested the system on FIRE 2011 SMS based FAQ retrieval corpus. Results seems encouraging.

Author: Srinaga, Nikhil N
Title: Design of a Novel High Linearity Down Conversion Mixer for GSM Band Applications
Supervisor: Gupta, Sanjeev
Call No.: 621.3845 SRI
Acc. No.: T00356
Keywords:
Abstract: Double balanced Gilbert cell mixer (GCM) is the mostly used kind of mixer as it provides conversion gain and has port to port isolation. This mixer lacks in linearity and noise figure which are to be taken care in designing mixer. Linearity is important for mixer design, to get an undistorted signal at its output. Similarly noise figure of double balanced GCM is more due to more number of components and is to be decreased to add less noise to RF signal. To increase the linearity of mixer, necessary changes are to be done at transconductance stage. The linearity of the mixer proposed is increased, by making use of an additional capacitor in parallel to gate capacitance and derivative superposition method. Derivative superposition method needs more number of transistors at transconductance stage resulting in increase of parasitic capacitance, resulting in an increase of flicker noise from indirect mechanism. This flicker noise due to parasitic capacitance is reduced by placing a tuned inductor in parallel to it.

Author: Timbadiya, Jaykant (201011040)
Title: FPGA Implementation of Multiband and Multimode Modem for Software Defined Radio(SDR)
Supervisor: Dubey, Rahul
Call No.: 621.384 TIM
Acc. No.: T00368
Keywords:
Abstract: Now a days Software Defined Radio(SDR) is becoming popular for wireless communication because of it's flexibility to change as per requirement through software. The work presented here describes the different methods of designing a Multiband and Multimode MODEM, implementation on programmable device like FPGA and verification for different functionality and specification. The design presented here has ability to switch between different modulation scheme and different data rate. Multiband and Multimode modem includes BPSK and QPSK modulator and demodulator with Forward Error Correction and other base band processing.

Author: Tiwari, Sandeep Kumar (201011043)
Title: Design & Layout of a Low Voltage Folding & Interpolation ADC for High Speed Applications
Supervisor: Sen, Subhajit
Call No.: 621.3815 TIW
Acc. No.: T00370
Keywords:
Abstract: Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC) plays a vital role in mixed analog signalling, communication and digital signal processing world. Now a day, the demand for designing of high speed, low power and low voltage ADCs are increasing tremendously in high speed data processing applications. In the folding and interpolation ADCs folding amplifiers have the serious bandwidth limitation problem because of larger parasitic capacitance and resistance at the output node. In this thesis work a low voltage and

high speed folding and interpolation ADC is implemented using current steering CMOS folding amplifier followed by transresistance amplifier (TRA) in UMC 180nm CMOS technology. The current steering folding amplifier significantly reduces power as well as number of tail current sources compared to the conventional folding amplifier. Transresistance amplifier, which is connected at the output of folding amplifier, avoids the analog bandwidth limitation problem. MSB and LSB bits are generated simultaneously at the output therefore sample and hold circuit is not required in this architecture. This proposed circuit works at 1.8V power supply and 85 MSamples/S and consumes 70mW power. Simulation and Layout of Folding and Interpolation ADC were done using UMC CMOS 180nm technology in the Cadence Analog Design Environment.

Author: Topiya, Vishal N. (201011029)
Title: Carrier Recovery In Software Defined Radio (SDR)
Supervisor: Dubey, Rahul
Call No.: 621.38216 TOP
Acc. No.: T00361
Keywords:
Abstract: The work presented here, deals with the carrier synchronization in digital communication system. The transmitter and receiver are two separate circuits located at a distance end and rarely share same carrier frequency oscillator and hence it required to synchronize these two carrier frequency oscillator. This task is performed by the circuit called carrier recovery at receiver end. In this document, different sub modules required to implement carrier recovery structure at receiver end is discussed in detail and each sub module is tested separately using Xilinx® ISE tool. Then these sub modules are used as black boxes, to realize complete carrier recovery structure in Matlab Simulink® tool. By using Matlab Simulink® tool one would get better idea of signal processing at each stage of the carrier recovery structure. Then this complete carrier recovery model of Simulink® is translated to Modelsim® model and verified for functionality. Here this carrier recovery model is used for Software Defined Radio (SDR) application so the complete model of SDR is realized in Matlab Simulink® environment and recovered carrier is used for demodulation part of the SDR.

Author: V, Harikumar (201011016)
Title: Multiresolution fusion using compressive sensing and graph cuts
Supervisor: Joshi, M.V.
Call No.: 621.367 HAR
Acc. No.: T00351
Keywords:
Abstract: Multiresolution fusion refers to the enhancement of low spatial resolution (LR) of Multispectral (MS) images to that of Panchromatic (Pan) image without compro- mising on the spectral details. Many of the present day methods for multiresolution fusion require that the Pan and MS images are registered. In this thesis we propose a new approach for multiresolution fusion which is based on the theory of compressive sensing and graph cuts. We rst estimate a close approximation to the fused image by using the sparseness in the given Pan and MS images. Assuming that the Pan and LR MS image have the same sparseness, the initial estimate of the fused image is obtained as the linear combination of the Pan blocks. The weights in the linear combination are estimated using the l1 minimization by making use of MS and the down sampled Pan image. The nal solution is obtained by using a model based approach. The low resolution MS image is modeled as the degraded and noisy version of the fused image in which the degradation matrix entries are estimated by using the initial estimate and the MS image. Since the MS fusion is an ill-posed inverse problem, we use a regularization based approach to obtain the nal solution. We use the truncated quadratic prior for the preservation of the discontinuities in the fused image. A suitable energy function is then formed which consists of data tting term and the prior term and is minimized using a graph cuts based approach in order to obtain the fused image. The advantage of the proposed method is that it does not require the registration of Pan and MS data. Also the spectral characteristics are well preserved in the fused image since we are not directly operating on the Pan digital numbers. Effectiveness of the proposed method is illustrated by

conducting experiments on synthetic as well as on real satellite images. Quantitative comparison of the proposed method in terms of Erreur Relative Globale Adimensionnelle de Synthse (ERGAS), Correlation Coecient(CC) , Relative Average Spectral Error(RASE) and Spectral Aangle Mapper(SAM) with the state of the art approaches indicate superiority of our approach.

Author: Bhatt, Prakruti Vinodchandra (201011019)
Title: Low Complexity 2-Level (FFT-GOERTZEL)SpectrumSensing Method for Cognitive Radio
Supervisor: Chakka, Vijaykumar
Call No.: 621.384 BHA
Acc. No.: T00354
Keywords:
Abstract: Energy detection in frequency domain is a preferred technique for the spectrum sensing and the accuracy of frequency estimation depends on the Discrete Fourier Transform (DFT) size. Instead of computing full length (N) DFT of the whole data, a new two level (coarse-fine) technique for energy detection is proposed. In the first (coarse) level, time averaging of smaller size (L<<N) data blocks of the whole data and its DFT are computed and Neymen Pearson based detection is performed to determine the presence of energy in the subbands. In the second level (fine), Goertzel algorithm is applied to determine the fine estimates in those subbands. Matlab based experiments are performed to verify the performance of proposed method in terms of probability of correct detection and false alarm at different noise levels. Simulation results show that this method can be applied for non-uniformly occupied spectrum also. The complexity of this approach is evaluated and it is 51% computationally more efficient for the considered case. Different windowing methods have been evaluated to be used for better detection performance. It is shown that optimal Discrete Prolate Spheroidal Sequence window helps in minimizing the spectral leakage to the adjacent bands, hence reducing false alarms and improving frequency estimation for Cognitive radio. Adaptive thresholding methods have been applied to the proposed detection method for increasing the reliability of spectrum sensing and combating the problem of noise uncertainity. Directions to extend the work further for case of Multipath fading environment and spatial sensing have also been mentioned in the thesis.

Author: Vora, Manali (201011005)
Title: Texton based auto region detection forImage inpainting
Supervisor: Joshi, Manjunath
Call No.: 621.367 VOR
Acc. No.: T00343
Keywords:
Abstract: Historical monuments are considered as one of the key aspects for modern communities. Unfortunately, because of variety of factors these monuments are sometimes damaged or destroyed. Image inpainting is the process of restoring the damaged image and hence can be used as a useful tool for restoring the images of historical monumnets. Inpainting techniques developed so far require the user to manually select regions to be inpainted. In this thesis, we propose a novel approach for automatic region detection for inpainting. Given a frontal face test image and a set of face images of monument consisting of vandalized and non-vandalized regions, our task is to: 1. extract potential regions of interest like eyes, nose and lips, 2. identify whether a particular region is vandalized or not and 3. inpaint the vandalized regions using the available non-vandalized regions. In our approach, potential regions of interest are rst localized using the bilateral symmetry based method, while the identication of vandalized and non-vandalized regions is done based on the texture statistics. The texture statistics are obtained by extracting the textons from the lter response space by using the K-means algorithm. After identifying vandalized regions, Poisson image editing technique is used to inpaint them using the non-vandalized regions available either in the same image or from the other images in the database. Novelty of our approach lies in 1. automatic detection of target regions for inpaiting and 2. automatic selection of optimum number of textons. Experiments conducted on the frontal face images of monuments downloaded from the Internet give promising results.

Author: Yadav, Anshu (201011001)
Title: Modeling and Detecting Attacks Against Key Agreement Protocols
Supervisor: Mathuria, Anish
Call No.: 005. 82 YAD
Acc. No.: T00340
Keywords:
Abstract: Key agreement protocols establish a shared secret key between two or more communicating parties willing to exchange data over insecure channels using symmetric key cryptography. Based on the number of members involved in the communication these protocols can be classied as a two party or group key agreement protocols. Various formal methods are available in the literature to analyze the security of such protocols. This helps in establishing the validity of any attacks, if found, or to prove the security of the protocols under given adversarial assumptions. In this thesis we analyze the security of several existing two party and group key agreement protocols. We used provable security models like eCK'08 and enhanced eCK and the DS model given as an algebraic approach by Delicata and Schneider to analyze a class of DH based key agreement protocols. The distinguishing feature of key agreement protocols from key transport protocols is that the former aims to ensure the contribution of all the honest participants so that no one can predetermine the key. In a poorly designed protocol, an insider adversary can control the key in different forms as dened by Pieprzyk and Wang. This type of attack is termed as key control. We also dene ephemeral key control w.r.t. dishonest insider where it is assumed that the adversary also knows the ephemeral secret of the victim honest participants. This assumption is based on several advanced attributes that assume ephemeral leakage. We analyze this attack on MTI protocols using DS model. We have shown weakness in some provably secure two party implicitly authenticated protocols and modeled the attacks in provable security model. We also analyzed key control in some group key agreement protocols. We have used the DS model to formally derive an attack shown by Pieprzyk on Burmester-Desmedt protocol and have also proposed attacks on static version of the group key agreement protocol proposed by Dutta and Barua.

M. Des. Projects
(Abstracts)

2004-2006

Author: Desai, Nikita (200414003)
Title: Kite flying: an Indian experience; 90 p.; 2006.
Supervisor: Pandya, Vishvajit; Mazumdar, Madhumita and Gupta, Anirban Dutta
Call No.: 796.15 DES
Acc. No.: T00133
Keywords: Kites--Juvenile literature;Kites; Kite flying—India.

Abstract: Chapter 1: Introduction

Chapter 2: The culture of kites

Chapter 3: The aspects of kiting

Chapter 4: Putting it together

Chapter 5: The Movie as a Guide

Chapter 6: The Interactive

Chapter 7: Conclusions

Notes

References Cited Sources

Author: Khetan, Lokesh (200414001)
Title: Utensils museum; 70 p.; 2006.
Supervisor: Pandya, Vishvajit and Gupta, Anirban Dutta
Call No.: 739.5 KHE
Acc. No.: T00132
Keywords: Art metal-work – India; Implements, utensils, etc. – India; Implements, utensils, etc. -- India -- Gujarat.

Abstract: Chapter 1: Museum displays

Chapter 2:The veechar utensils museaum

Chapter 3: Utensils and their contets

Chapter 4: Objectives of the project

Chapter 5: The special utensils

Chapter 6: Digital multimedia aspects

Chapter 7: Utility of project

Chapter 8: Outcome and variation

Chapter 9: Search for topic

Chapter 10: Selection of utensils

Chapter 11: Research and data collection

Chapter 12: Planning the Shoot

Chapter 13: Interface design

Chapter 14: Illustrations, design aspects and image gallery

Chapter 15: Loading

Conclusion

Author: Saraswat, Manish (200414005)
Title: Re-telling panchatantra: an attempt to rediscover the relevance of panchatantra tales in today's society; ix, 34 p.; 2006.
Supervisor: De, Kuntal and Sarkar, Aditi Nath
Call No.: 398.24520934 AGA
Acc. No.: T00135
Keywords: Fables, Indic; Tales—India; Fables of Bidpai; English; Panchatantra Fables; Indic -- History and criticism; Politics in literature.

Abstract: Current trends in the field of education show people's high motivation 10 take up initiatives for their children to get them educated through the new medium of computer based learning.

Teaching and learning practices are taking new shapes with the development of" new medium of communication. This medium allows the children to learn on their own, in a way that engages their interest. The acceptance of this form of education is achieved by the integration of essential social values and the roots of Indian heritage with all the disciplines taught to the children as they are seen vital to develop the skills and knowledge sets which primary students lack due to the excessive lime spent with computers in the name of education.

Moreover this new medium is open to exploration, and since there is no guidance, the vulnerable children do not understand where and at what point they arc learning and when (hey need to slop; it can be said that this medium is not without its pitfalls.

This medium also has another side effect; that it alienated the children from their grand parents and the traditional way of story telling as a form of learning.

Thus there is a need for design that instructs the child sifting on a computer to learn about the real world in a form which uses the capabilities integrating the old methods of story telling with the newer more exciting digital media that (he children are drawn to and enjoy.

Author: Tatawawadi, Prachi (200414004)
Title: Point it: a visual aid; 51 p.; 2006.
Supervisor: De, Kuntal and Gupta, Anirban Dutta
Call No.: 915.4045475 TAT
Acc. No.: T00134
Keywords: Gujarat (India) –Guidebooks; Tourist Guides.

Abstract: Chapter 1: The problem

Chapter 2: The visual language system

Chapter 3: Relevance

Chapter 4: The guide book

Chapter 5: Objectives

Chapter 6: Features

Chapter 7: Planning & execution

Chapter 8: Go mobile

Chapter 9: Mobile phone version

Chapter 10: Mobile Navigatio structure

Chapter 11: Forming visualo sentences

Chapter 12: Multimedia concepts

Chapter 13: Application & utilization

Chapter 14: Expected outcome

Chapter 15: Future prospects

Chapter 16: Drawbacks

Chapter 17: References

Notes

Author: Ujawane, Anand (200414002)
Title: Vehicle Katha: a 2d stop motion animation film; 54 p.; 2007.
Supervisor: Mazumdar, Madhumita; Sarkar, Aditi Nath, and Gupta, Anirban Dutta
Call No.: 791.4334 UGA
Acc. No.: T00136
Keywords: Animated films; Cinematography, Abstract; Experimental films; Experimental films -- India -- Gujarat.

Abstract:

- Vehicle katha - a 2d stop motion animation film.
- 'Take care of your vaahans and they will take care of you' - a public interest message about vehicle h. maintenance.
- The film uses the vaahan of the Mother Goddesses of Gujarat as metaphor to communicate the importance of vehicle in everyday life.
- The film is presented as folklore. It uses folk art -mata ni pachedi as the visual treatment and folk music - daayaro as background sound.
- Duration of the film - eight minutes.

2005-2007

Author: Ahalpara, Ami (200514003)
Title: Bhavai on bhavai; 50 p.; 2007.
Supervisor: Sarkar, Aditi Nath; Gupta, Anirban Dutta; De, Kuntal; Mazumdar, Madhumita; Pandya, Vishvajit
Call No.: 791.4372 AHA
Acc. No.: T00138
Keywords: Feature films; Folk dancing India; Folk Tale; Bhavai

Abstract: The starting point for this project was the premise that folk arts are perishing and they need to be preserved. However while reading some of the leading researchers' works, it was realized that there were counter views also. In the present days of modernization and globalization (where physical boundaries are diminishing at a faster pace), no tradition can remain in isolation preserving its purest form for a sufficiently long time. Changes as per the forces from within the society are inevitable. I took an example of one such folk tradition, called Bhavai, studied it from a researcher's point of view and finally realized that though its original form and intent are more or less lost, some of its elements have survived. To communicate this idea, I chose the medium of film. The film called Bhavai on Bhavai poses the question, whether tradition is eventually lost or it transforms itself into other forms. It does not give a clear-cut answer to the main question, but finally leaves it to the viewers to judge it for themselves.

Author: Gulatee, Nidhi (200514001)
Title: Inside a weekly haat- impressions from Chhota Udaipur; 78 p.; 2007.
Supervisor: Sarkar, Aditi Nath; Mazumdar, Madhumita; Pandya, Vishvajit; Gupta, Anirban Dutta and De, Kuntal
Call No.: 381.10265095475 GUL
Acc. No.: T00139
Keywords: Marketing – India; Rural marketing – India; Retail trade – India; India -- Rural conditions; Bazaars; Chhota Udaipur; Weekly Haat.

Abstract: In- project "Inside a Weekly Market- Impressions from Chota Udaipur," is a study of a rurual market of India.

This project focuses on the pattern of the social organization of the sellers in the haat of Chhota Udaipur near Vadodara. The Final product shows how in this modern world of constructed shops even there is a traditional market that sets up for one day each week.

With the sue of Hyper- media an attempt has been make the haat alive to the user with the help of video, photographs and digital drawings, narration, sound and text.

The project can be used by tourism industry, sociologists, scholars and people interested in knowing village markets.

Author: Kumawat, Sumit (200514002)
Title: Pichhvai ke pichhey; 48 p.; 2007.
Supervisor: Mazumdar, Madhumita and Gupta, Anirban Dutta
Call No.: 751.709544 KUM
Acc. No.: T00137
Keywords: Textile painting -- India – Rajasthan; Decorative arts -- India – Rajasthan; Textile fabrics -- India – Rajasthan; Nathdwara.

Abstract: The Project is an attempt to explore beyond the evident. It imparts the knowledge about the utilization of background that gives context to foreground.

The Art form of Picchvai (Painted backdrops of Nathdwara) as a specific technique of Visual communication is chosen as the main research area. It explores the traditions and philosophy associated with it in the context of Nathdwara.

The vast ethnographic work allowed broadening of the context and analyzing various other popular visual and performative traditions of the region viz. Kathputli, Bhopaji ki katha, Ajooba, Nathdwara Studio photography, etc. These traditions primarily use the background to create a sense of darshan (spectacle) for the viewer. It further includes the contemporary mode of communications such as Photography, advertisements, etc.

This knowledge has been imparted to the user through an (Hypermedia) interactive multimedia CD ROM. The Hypermedia format allows the user to seek through the inter□woven medias so as to get a clear picture of the subject. It allows him/her to understand the complexities and simultaneously apply the learning. Thus, it creates the space for the viewer where at one moment he can be an observer while at another he is a performer.

Author: Padia, Bhakti (200514005)
Title: City flavours; 53 p.; 2007.
Supervisor: Mazumdar, Madhumita and Gupta, Anirban Dutta
Call No.: 641.595475 PAD
Acc. No.: T00141
Keywords: Food habits – Gujarat: Food customs – Gujarat; Indian cookery; Indian cookery – Gujarat; Flavor; Farsaan; Food additives; Food consumption; Cost and standard of living food supply.

Abstract: 'City Flavours' is a multimedia project, which intends to communicate the idea of 'reconciliation of tradition and modernity in the city of Ahmedabad' through the eating culture of its citizens. While the story is being told using food, the main focus remains on farsaan as a popular category of Gujarati cuisine. The message is conveyed through the medium of a documentary film, which is supplemented by a brief interactive segment.

This document is a compilation of the design process followed in the making of 'City Flavours'. I have divided the document in two main sections – Research and Implementation. The Research talks about collecting and analyzing the content for the product. It describes the procedure followed in deriving the concept and linking together of accumulated information in order to create knowledge. The Implementation describes the manner in which various mediums are used to communicate the idea.

Author: Singh, Rashmi (200514004)
Title: Well of meanings: an insight into the step wells of Gujarat; 50 p.; 2007.
Supervisor: Sarkar, Aditi Nath; Gupta, Anirban Dutta; De, Kuntal; Mazumdar, Madhumita and Pandya, Vishvajit
Call No.: 725.9 SIN
Acc. No.: T00140
Keywords: Stepwells--India—Gujarat; Water and architecture--India—Gujarat; Architecture, Hindu--India—Gujarat; Sculpture, Hindu--India—Gujarat; Gods, Hindu, in art.

Abstract: Stepwells of Western India were often regarded as magnificent architectural solutions to the seasonality of water supply in the region. But as this multimedia presentation will show, the stepwells were much more than architectural wonders. They are laden with a whole range of meanings which derive from historical myths, meanings, beliefs and practices of the people of the region in which they were built. The presence of water in a stepwell made them the active focal point in villages.

There was a time when these stepwell were used by the people for satisfying different requirements. This made the presence of the stepwell inevitable in their lives. However, because of the changes in climatic conditions, almost all of the stepwells are now dry, creating a distance between the stepwell and the user as the real purpose of stepwells is being lost. The stepwells are losing their original contexts with their real purpose and hence their importance in lives of people.

The Stepwells of Gujarat are becoming important subject of public attention in recently. Their importance as site of water management is being complimented by appreciating their potential as attractive sites for cultural tourism in Gujarat. Stepwells are unique feature of Gujarat. Their distinctive style of architecture and ornamentation takes us to a new world of discoveries. At the same time, the multitude presence of the stepwells in the western part of the country opens the

door of knowing their larger social and cultural contexts.

The focus of the project is to study the stepwell of Adalaj to understand larger social, historical and cultural context and then make sense of the multiple cultural meanings attached to these wells in Gujarat. Since the Adalaj stepwell does not stand in isolation but there exist a number of other stepwells in this region. Hence, through this thesis, an effort has been made to build up the connection of the local context of the stepwell with regional.

2006-2008

Author: Agarwal, Nidhi (200614001)
Title: VIKALP: aware a child – save childhood; 75 p.; 2008.
Supervisor: Raje, Nitin
Call No.: 362.76630715 AGA
Acc. No.: T00187
Keywords: Child abuse -- Reporting -- Study and teaching (Continuing education) – India; Child care – India; Educational equalization -- India. Adult education – India; Continuing education – India; Children with disabilities -- Rehabilitation -- Study and teaching; Infants -- Rehabilitation -- Study and teaching; Health Personnel -- education -- collected works; Education, Continuing -- collected works; Child Development Disorders -- prevention & control -- collected works;
Child, Exceptional -- collected works.

Abstract: The focal points of the project are street children, who are being exploited at different levels and under different circumstances. Keeping this in focus and going through the readings and research works done in this area, it was realized that there are many deep-rooted problems both at personal and social level which all together creates unfavorable conditions for children that spoil their childhood.

Lot of amendment has been made in constitution but the problem still persists and the percentage is increasing at a regular scale. To address the problem effectively it has to be analyzed in a right manner and direction with sincerely and collectively affords by NGO(S), area panchayats, district administration, state and central government.

Among so many problems with which children are fighting for their survival "The Child Labour" (age group 7 to 14 years, who are engaged in hazardous and other gainful occupations which are injurious to their health anddevelopment) is one such problem that plays an important role in departing children from enjoying their childhood. It's not just parents, teachers, factory owners and at large the society, who has to understand the hazardous effect of child labour, rather children themselves should be made aware of the importance of education in their life to solve the problem at grass root level.

To communicate this idea, I choose the medium of film, a film that has a social appeal to make, it interest children and have much-much effect on their soft, unspotted and plain mind. The dialogue, body language, gesture are powerful medium of communication and has a long lasting impact as well.

To make the product more effective their should be some group activities in which the children are asked to talk about what they had seen in the film, doing such discussions they will think about the whole subject again and again and for this I had design a colouring book that will be given to the children after they had seen the film, in which the children had to colour the sketches as they had seen in the film. Each sketch is supported with a question which has to be answered as per the story. This will be group activity and a best medium to communicate and interact at different levels.

One such film is "Vikalp" that put forward the story of two boys from similar background. One of them, who is comparatively an intelligent boy got attracted towards easily available money, good food and end up joining work on a road side shop to fulfill his unwanted needs whereas the other, who is comparatively less intelligent listened to his teachers, parents voice and continue education, and at last turned out to be much happier in the latter course of life.

The story of the film is moving around the real-life situation of society thus screening two ways of dealing a situation. It poses question for the viewers (i.e. children, parents, teachers, shop owners and society in large) at different levels.

Author: Bhar, Rahul (200614008)
Title: Waterpoly: a learning game kit; 68 p.; 2008.
Supervisor: Raje, Nitin

Call No.: 333.9116 BHA
Acc. No.: T00191
Keywords: Soil science; Water conservation; Water conservation – Technique; Water harvesting – Technique; Computer Aided Design.

Abstract: The title of my project is "Waterpoly" – A Learning Game Kit. The objective of my project is to design an interactive computer aided training program to bring awareness of Water Conservation methods for improving standard of living in rural India.

My product contains a Board Game and an Information CD.

The board game is based on simulation of agricultural inputs required to cultivate rice. This is to arouse curiosity and provide an experienced based learning.

Another part of the project is the Information CD. The Information CD provides the information regarding various water conservation methods used within the game and its related sub domains like rainfall, soil, watershed etc. Detail description and implementation methodologies for water conservation are also included in the CD as an extra level of knowledge.

Along with the information for the various water conservation methodologies, there is a game help within the CD, to help a player to understand how to play a game and acts as a tutorial for the game.

Author: Dubey, Smita (200614006)
Title: Verbs in the Jungle; 23 p.; 2008.
Supervisor: Desai, Binita
Call No.: 371.91233 DUB
Acc. No.: T00190
Keywords: Vocabulary -- Study and teaching; Deaf children – Language; Deaf children -- Education (Preschool) – Language; Hearing impaired children – Language; Hearing impaired children – Education; Hearing impaired children -- Education (Preschool) Hearing impaired children -- Education – India; Hearing impaired children -- Language -- Ability testing; Deaf -- Education – India; Speech therapy for children; Audiology; Intonation (Phonetics) Speech perception in children.

Abstract: Project is based on vocabulary development of hearing impaired children these children do not have hearing sense and because of that, they are unable to speak Understanding about various things is different for a child with hearing disability as compared to normal child Because of that, the teaching methods are different for them. In the initial stage of education for kids with hearing disability, parents and normal school teachers do not know how to teach the child The main problem is that hearing disabled child does not have a language vocabulary According to psychologists when a child without hearing disability starts going to the school, he has at least more than 3,000 words language vocabulary. However, in case of hearing disabled child, he does not have early age vocabulary The main target of the project is to help a hearing impaired child build his vocabulary In the early age.

Author: Kadam, Neha (200614004)
Title: Urban soundscapes: an exploration of why and how, we hear, what we do…; 49 p.; 2008.
Supervisor: Mazumdar, Madhumita
Call No.: 306.4842 KAD
Acc. No.: T00188
Keywords: Cities and towns; Urbanization; City and town life; Soundscapes Folk music -- India --History and criticism; Music and globalization – Finland; Sounds in literature; Sound -- Recording and reproducing -- Great Britain -- History -- 19th century; Speech in literature; Sound in literature; Voice in literature; City and town life in motion pictures; Music -- 21st century -- History and criticism; Music and technology; Popular culture -- 21st century.

Abstract: Urban soundscapes is a multimedia exploration of the forms, practices and habits of engaging with sound in a contemporary urban Indian context. It focuses on the listening habits of a section of the urban Indian youth and invites critical reflection on the choices they make in the selection and enjoyment of the sounds that come to them through the mediation modern technology.

Put simply, Urban Soundscapes is both an exploration and reflection on why we hear what we do as we live our lives in the complex sonic environment of the modern city.

It begins on the premise that the urban soundscape is not a random collection of sounds. Sounds in the city come in forms, patterns, designs and shapes that are tied to dominant economic structures and local cultural contexts.

It invites the user to explore this observation through four different points of entry through technology, through the consumer, the music market and of course through the makers of music themselves. The role of technology in creating a complex and evolving urban soundscape is underscored by a focus on the particular forms, tastes, and habits of listening to music by a dominant section of the urban Indian youth.

Based on both fieldwork and academic writings on the subject, this product tries to present a complex cultural and social phenomenon in a format that tries to appeal to both the initiated and informed. It can in a sense position itself as educational software that tries to complement serious writing on the subject by putting together the constitutive elements of multi□media on a digital medium that is both attractive and affordable.

It does not in any way pretend to be either a comprehensive or definitive work on the subject. It offers instead the possibility of generating a critical awareness of one's social and cultural context in a way that is both intelligible and entertaining.

Author: Kore, Manasi (200614010)
Title: Khel Mangalagauriche: women and somatic recreation; 40 p.; 2008.
Supervisor: Desai, Binita
Call No.: 394.3095479 KOR
Acc. No.: T00192
Keywords: Manners and customs; Games with music; Traditional games; Customs and practices -- Maharashtra – India; Maharashtra culture; India -- Social life and customs; Folklore -- -- Maharashtra -- India.

Abstract: In Maharashtra, there are many rituals and festivals celebrated especially by women. The reason behind performing such rituals is to worship a god or goddess. But the women themselves are benefited from these rituals. The traditional games are no exception. Maharashtra has a rich tradition of games for women, played in the festivals. They are performed throughout night to entertain the Goddess. But these games take care of the women's mental as well as physical health.

The traditional games played in a community represent the culture of that community. Mangalagaur games, played by Chitpavan Brahmin community of Maharashtra are one of the most popular games found. The games involve physical activities synchronized with songs. Song and exercise together can be compared with the aerobics. Though Mangalagaur is celebrated only by Brahmins of Maharashtra, similar games can be seen played on different occasions like Nagpanchami, Hartalika and Bhondala in other communities. 'Khel Mangalagauriche' (Games of Mangalagaur) is an attempt to understand the importance given to a woman's mental and physical health in the Maharashtrian culture through the games played during the Mangalagaur.

Author: Patel, Bhavesh (200614005)
Title: Moving canvases: truck as a new medium; 47 p.; 2008.
Supervisor: Sarkar, Aditi Nath
Call No.: 709.540905 PAT
Acc. No.: T00189
Keywords: Art appreciation; Trucks – Painting; Painting – Indonesia; Street art – Indonesia; Trucks – Decoration; Automobiles – Painting; Trucks in art; Trailers in art; Visual communication -- Social aspects; Art, India.

Abstract: The most common sight of daily life in India consists of the omnipresent truck that travels on the highways all across the nation. For everybody on the road, truck is a commonplace sign of thriving overland transport industry, and for many a momentary pause of appreciation of the wooden

structures on the wheels covered with clashing motifs. A striking vision on the roads of India is the vision of truck covered in a riot of color and design. These monstrous vehicles are better known for clogging traffic then for their aesthetic qualities. There are three million trucks in India. Perhaps the biggest paradox of truck art is that despite its commonness most people do not recognize it as art. Truck art like movie banners, advertising and posters, is a popular medium that expresses the creators thoughts. It is a popular form of art that is self advertising and propagating one, which has no single artist, which is regional yet universal, which is exposed to masses.

I want to look in to the concept of usage of paintings and the decorations done on the trucks in the specified domain of art. So through this project I want to show the importance of visual representation in popular culture by focusing on the decorations done on the truck. It is an attempt to go beyond the basic characterization of art and look in to how forms of art convey identity in society through this mode of visual communication.

Author: Abhineet Kaur, Virdi (200714008)
Title: What Child Art Could Say?; 39 p; 2009.
Supervisor: Mazumdar, Madhumita
Call No.: 372.52 KAU
Acc. No.: T00233
Keywords: Child artists; Child psychology; Art – Psychology; Children as artists; Creative thinking (Education); Child development; Creative ability in children -- Art.

Abstract: "What child could say?" is project which intents to design a communication of public interest message for middle class urban Indians. It is to alert parents in the direction of importance of family peace and harmony. And to be sensitized to the impact of domestic conflict on there children in the family. It is a message in which a child drawn image is made to say to the adult's world for not letting him grow in a place that is dark and unconstructive rather provides an environment which is bright and blissful for them to grow.

Author: Alex, Abin (200714001)
Title: Christianity And Kathakali Dance- Drama Of Kerala; 40 p.; 2009.
Supervisor: Sarkar, Aditi Nath
Call No.: 793.3195483 ALE
Acc. No.: T00228
Keywords: Kathakali; Dance – India; India -- Social life and customs; Christianity -- India -- Kerala.

Abstract: Kathakali and Christianity have long been associated with the state of Kerala. Both have had their own independent identity. Since Kathakali was not an art form that portrayed the Biblical stories and it was confined within the temple compound, in the early years an intermingling of them was a question out of context. Though Christians in Kerala are known to have co-existed with native culture of Kerala, the arrival of Portugese and strict rules imposed by the Christian orthodox authority saw the community taking less to the native culture. This resulted in the formulation of new art forms exclusively belonging to the Christians of Kerala like Margamkali and Chavitunadakkom. Moreover, the mythological stories that are part and parcel of Kathakali performance where considered to be chiefly belonging to Hindus. There were rites and rituals before, during and after the performance of Kathakali that led people from non-Hindu community to make unfriendly them from the art form. It was not until the 1960s that the ruling of the second Vatican council and the efforts of people to make Kathakali represent Kerala rather than a particular division, those stories from Bible made their way into the literatures of this dance form. This development is recent comparing with the time these two entities have been existing in Kerala. There is the need for familiarizing the masses about this as the growth of this segment of Kathakali is oblivious to a lot of people. I intend to meet this end through this project.

Author: Anglay, Hemang (200714004)
Title: Darshan On The Highway Urbanisation & Popular Religion in Contemporary Ahmedabad; 35 p.; 2009.
Supervisor: Pandya , Vishvajit
Call No.: 388.1095475 ANG
Acc. No.: T00231
Keywords: Highway research; Roads -- India -- Gujarat – Ahmedabad; Environmental impact analysis -- India -- Gujarat – Ahmedabad; Traffic safety – Research; Road transport ; Roads -- Design and construction; Highway departments -- Washington (State) – Periodicals; Highway planning -- India -- Gujarat -- Ahmedabad.

Abstract: Darshan on the Highway is a multimedia news story which is incorporated in a news website. It brings out the quality and characteristics of New SG Highway. In the recent years a new lifestyle has emerged on account of growing economy around the city of Ahmedabad. Two major forms of structures which emerged are the 'Temples' as well as the 'Business' complexes. Mainly the religious structures and business structures are the two main segment which share a symbiotic relationship between them, and also constitutes to the Visual Display of the entire stretched area. It has changed the economics of this stretch of the city making it a hub of a range of malls, multiplexes and restaurants. The temple complexes along with shopping complexes make the SG Highway a unique site for the study of the nature of urbanization and popular religious practice in contemporary Gujarat. It brings out the recent change which has transformed into a cultural phenomenon - The co-existence of economic enterprise and spirituality. It deals with the demands of work, leisure and religiosity in the best possible ways. The SG highway has attracted both citizen and media attention in recent times because of its mushrooming temple complexes and replicas of popular shrines on pilgrim circuits. Keeping this exceptional feature as the driving force I have tried to create a multimedia presentation in a sequence which might open up the curtains one by one. A news feature on the SG Highway had already appeared in the Ahmedabad edition of the Times of India on the 24th of July 2003. At that point the temples complexes had just begun to take shape with the successful replication of the Vaishno Devi Temple. My news story brings the story down further to 2009 to show the more recent replication of the Tirupati Balaji temple. The news feed drives the user to explore the replicas of two major shrines one being from north and the other being from the south, as well as its implications in contemporary senario. Namely, the Vaishnavdevi temple and the Tirupati Balaji temple on SG Highway. Given the spatial limitations of the multimedia news format, I have chosen to depict some salient features of the SG Highway focusing in particular on the replica shrines and their significance for visitors and devotees in the city of Ahmedabad.

Author: Kaur, Gagandeep (200714003)
Title: Body Sense Towards A Sensible Approach To Health And Body Image; 25 p.; 2009.
Supervisor: Mazumdar, Madhumita
Call No.: 306.461 3 KAU
Acc. No.: T00230
Keywords: Body image in adolescence; Body image – India; Body image – Research; Self-perception – Research;. Body Image.

Abstract: Body sense is a website intended as a platform for young women to help them identify and respond to the conditions in their lives that contribute to their confused body images, eating disorders and related problems of obesity and depression. It seeks to send out the message that It is important to resist myths about obesity, thinness or the perfect body that the market sells the in order to embrace a healthy lifestyle and a positive body image.

Author: Kholia, Puru (200714009)
Title: Sons of Soil; 50 p.; 2009.
Supervisor: Desai, Binita
Call No.: 796.812095 4 KHO
Acc. No.: T00234
Keywords: Bodybuilding; Wrestling – India; Wrestling -- Social aspects – India; Wrestling – Folklore; India -- Social life and customs; Physical fitness; Physical education and training – India; Physical fitness – History; Country life -- India.

Abstract: An integral part of physical culture, Pehelwani prevails in India since ancient times and having undergone several changes, it still exists in a slightly different form however it is not as popular as it used to be a few decades ago. Pehelwani influenced the general lifestyle of many individuals, and for centuries it has been appreciated by the masses as the most popular form of entertainment. Certainly it is something which supports the formation of a healthy body residing I

a health conscious environment and it is for this reason Pehalwans are so passionate about the Akharas and their Gurus.

Author: Shah, Aneri (200714002)
Title: String Puppets of Rajasthan; 71 p.; 2009.
Supervisor: Raman, Sethu
Call No.: 791.530 954 SHA
Acc. No.: T00229
Keywords: Kathputli (Puppetry); Puppeteers -- India – Rajasthan; Marionettes -- India – Rajasthan; Community development -- India – Rajasthan; Puppet making; Puppets.

Abstract: The title of the project is "String Puppets of Rajasthan".

The Project is explores the contents of usage of background in the specified domain of the art form of Rajasthani Kathputli and their performers, Types of Puppet, Folklore stories about Rajasthani string Puppets, About Bhat Community, Story about first Net Puppeteer, History and myth about Vikramaditya's 32 dolls, Amar Singh Story about String puppets, Popular Modern Characters, How Puppeteer are Making the String puppets, Language of communication through Facial expression, Sutradhar, Boli & Team and stage, its Ritual customs and Traditions, and Modern trends. This project also sincerely appeals to all the generations to save this fabulous form of art.

The final output will an Interactive Multimedia CD- ROM which provides nonlinear access to multiple forms of information ranging from digital medium like film, sound, illustration, Photographs, interactive animation and text in a format that allows the user to explore it, and learn about the display principle in the context of Udaipur popular Folk Art Rajasthani string Puppet visual and Per formative traditions.

Author: Sharma, Neha (200714007)
Title: "Devo Athithi BhavaAthithi Devo Bhava" An event where God come in as Guest & guest comes as God'; 41 p.; 2009.
Supervisor: Pandya, Vishvajit
Call No.: 338.479 154 52 SHA
Acc. No.: T00232
Keywords: Tourism -- India -- Kulu Valley; Himachal Pradesh (India) -- Description and travel; Himachal Pradesh (India) -- Social life and customs.

Abstract: "Devo Athithi Bhava, Athithi Devo Bhava" is an exploration of a unique cultural phenomenon which leads to social, political and economical context of the place. It focuses on the festival "Dusshera in Kullu" where the Gods come as guests. The tourists i.e. guests who visit the place are also treated like God to the place. Project is basically to promote 'Tourism in Kullu' which is further exploration of not only the 'unique way of celebrating this festival but also communicates the "Impact of culture tourism" on and by the people of Kullu in Himachal Pradesh.

It invites the user to explore not only the culture and belief of the festival in the context of its celebration but also to assist the viewer to know about the local people and the place, where tourism potential provides the State, the tourist as well as the local people benefit, by organizing such culturally accepted festivals and events. Tourists are derived of opportunities to enjoy the rural, remote and the most scenic parts of the state due to lack of awareness. Thus, project explores them to find other places in the district those have equal cultural tourism potential. It generates critical awareness among the tourist who are visiting the place to get authentic information about the event.

It also gives information to the viewer about the culture diversity in India and gives knowledge of the tradition of celebrating dusshera festival in various parts of the country in different ways with independent history related to it.

Author: Sharma, Sparsh (200714010)
Title: Dhol di Awaaj; 30 p.; 2009.
Supervisor: Raje, Nitin
Call No.: 781.6254552 SHA
Acc. No.: T00235
Keywords: Folk music -- India -- Punjab; Popular music -- Social aspects; Bhangra (Music); Popular music -- India; Folklore -- India -- Punjab; Folk dance music -- India; Folk music, Panjabi; Folk songs, Panjabi; Sikhism -- Customs and practices; Folk art -- India -- Punjab; Punjab (India) -- Social conditions.

Abstract: Bhangra is a lively form of music that was Originated in Punjab region in Southeast Asia. Traditional is a fusion of music, singing & the beats of the dhol drum, a singled stringed instrument like: Iktara, Tumbi & Chimta. As it creating & expressing new identities in the globalizing world.

The idea is to communicate a cultural phenomenon as how Bhangra is transformed by Overseas Punjabis, As every one knows that bhangra got its own significance & place in culture of Punjab, India & Overseas as well as. Though it moves into mainstream culture & Punjsbi people have become more global & advance. Which effects on the second generation? How ever, the people who migrant from Punjab have had s effect on Western Punjabis & Now Bhangra have become global & gain popularity in Overseas as well. As I have diaspora are interpreting & expressing these new forms of culture. My more stress is the circumstance, conditions affecting the chance of people of Punjab and overseas also, who are forgetting their originality. Specially a second generation, they all like remix, thrilling songs, which have changed authenticity of bhangra. They like Punjabi songs, which got really its meaning. Even overseas Punjabis counterparts also come in motion by listening the beats of dhol even though they don't know the meaning of the lyrics. However I have taken up personal interviews of different types of people, interact with them, and finally I have divided three sections Rural Punjab, Urban Punjab and Diasporic Punjab. I have tried to show the changes have taken place with the pace of time. I have tried to compare the variations by audio, video, photographs, text and categorized the views of the people, personal interviews and Punjabi songs in form of multimedia design.

However, bhangra has brought the people of Punjab very close to non Punjabi communities, Though this is an achievement through which globally we have come together in Socially, Culturally and Religiously.

Author Index

Author Index

Author Index

Supervisor Index